U-matic

VIDEOCASSETE PLAYER

VP-5020/5040

THEORY OF OPERATION

SONY®

SERVICE MANUAL

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SECTION 1
VIDEO CIRCUIT

1-1. FOR VP-5020

1-1-1. RF Amplifier

The RF signal from the video head passes through the input transformer (T1 and T2), and amplified by FETs Q1 and Q2, whose S/N ratio is excellent. The resultant signal is fed to pins 23 and 24 of IC1 (CX134A). It is then sent through the head amplifier and RF amplifier to pins 16 and 17.

The CH-A and CH-B RF output signals are compensated in the middle range of their frequency response by capacitors and coils connected to pins 20 and 21. They are supplied from pins 16 and 17 of IC1, respectively.

Channel A is described below. This circuit contains a negative feedback loop between R7 and Q1. This feeds back the voltage from a voltage divider (R7 and R8). The peak value of the frequency response should reach 6 to 7 MHz, it is detected using an LC circuit (C7 and L2). If an unbalanced frequency response is caused by deviations between the heads for channels A and B, it can be adjusted using RV1. The RF output signal from pins 16 and 17 of IC1 is balanced using RV3. The resultant RF signal level is adjusted using RV4, and then passes through buffer Q4. The RF signal from Q4 passes through TP1 and high-pass filter FL1. The resultant Y RF signal is then sent to pin 14 of IC1.

Pin 15 of IC1 selects black and white. For the VP-5020, however, the color mode is fixed with pin 12 connected to ground.

The Y RF signal is passed through a Y RF amplifier and limiter in IC1. It is then passed through a dropout compensation switch. The RF signal with no dropout is fed from pin 4 of IC1 to Q5.

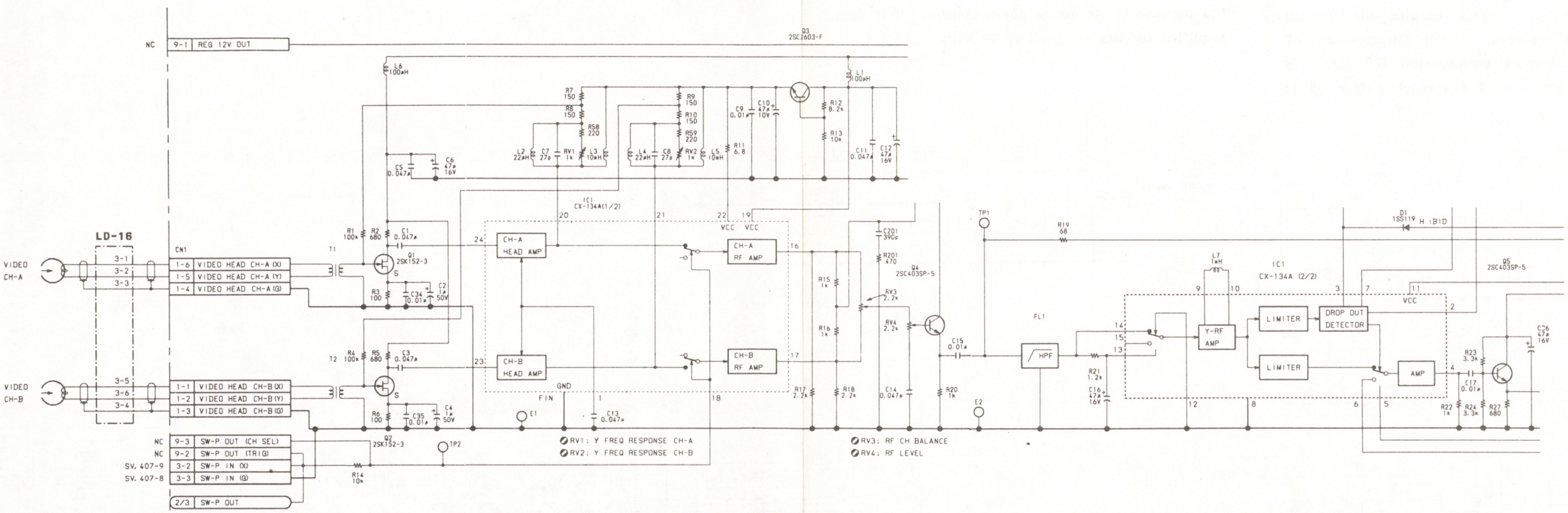


Fig. 1-1

1-1-2. Dropout Compensation Circuit

This is the circuit that inserts the 1H-preceding RF signal into the dropout portion of the RF signal.

Dropout is detected using an RF signal envelope detector (C21 and R45). Sensitivity is adjusted by changing the bias voltage of this circuit. The dropout detection sensitivity is determined by the input level at pin 14 of IC1 and is adjusted using RV5. A dropout pulse from pin 2 of IC1 turns on Q7, which provides hysteresis for the detection level. The muting switch of the dropout detector D1 is used to mute the dropout in the search mode.

The 1H-delayed signal is fed to pin 6 of IC1. The RF signal output from buffer Q5 is 1H-delayed using delay line DL2. When dropout is detected in IC1, the dropout compensation switch is set to the DROPOUT position. This enables the dropout portion to be replaced by the 1H-preceding RF signal. The dropout compensated RF signal is supplied from pin 4 of IC1 through buffer Q5 to pin 9 of IC5.

1-1-3. PB, Y RF Sideband Equalizer

During playback of a magnetic recording, overmodulation often occurs because the high-frequency signal level attenuates.

When the high-frequency RF signal level is low, the high-frequency signal cannot be demodulated completely, but is demodulated as a low-frequency signal. Black stripes appear on the monitor screen. Therefore, the high-frequency signal level is raised to prevent overmodulation.

The dropout compensated RF signal is passed through limiter IC5 (1/3) and sent from pin 6 of IC5. One of the resultant outputs passes through R32 and R33 and is sent to differential amplifier IC5 (2/3). The other output is fed through delay line DL1 to pin 4 of IC5. When the RF signal level is lowered, the signal at pin 4 is high-frequency boosted using differential amplifier IC5 because of its cosine characteristic. It is then amplified to obtain a peak of 10 MHz.

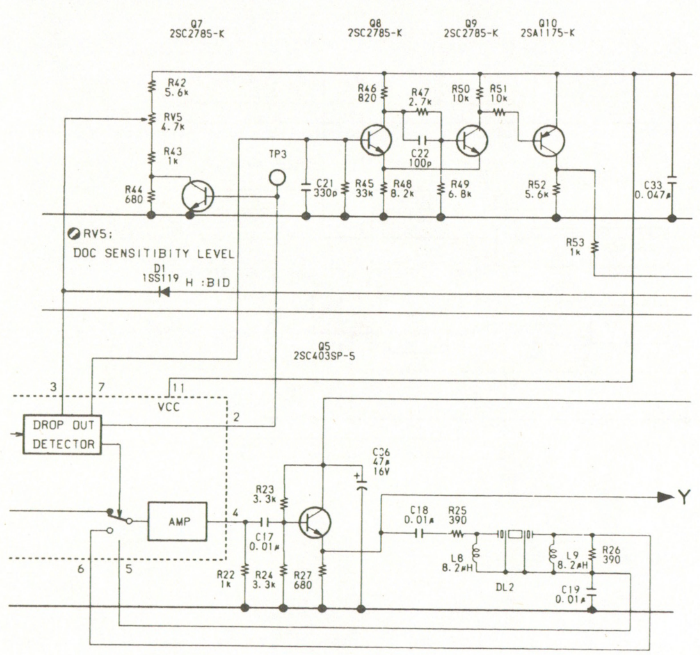


Fig. 1-2

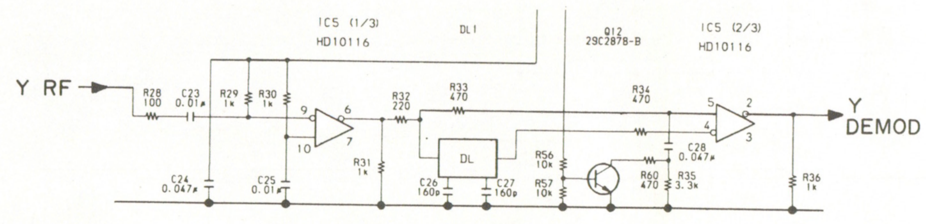


Fig. 1-3

1-1-4. Demodulator

The RF signal at pin 2 of IC5 is fed to pin 1 of IC2 and demodulated through a limiter. The demodulated video signal appears at pin 21.

The capacitor between pins 23 and 24 of IC2 determines the linearity of the demodulated signal. The output at pin 21 is passed through low-pass filter FL3 and becomes a demodulated video signal with the impedance of R102. The demodulated video signal passes through buffer Q101, and a deemphasis circuit (R104, R105, and C103).

The video level is adjusted using RV6 which is located at the emitter of Q102, so that the level at TP6 is 1Vp-p when the VIDEO OUT connector is terminated at 75 ohms. The output of the deemphasis circuit is sent through an equalizer (Q103 through Q106) to pin 12 of IC2 at approximately 250mVp-p. The resultant signal is passed through video amplifier IC2, and then is sent to pin 5 of IC2 at approximately 1Vp-p and to pin 4 of IC2 at approximately 2Vp-p.

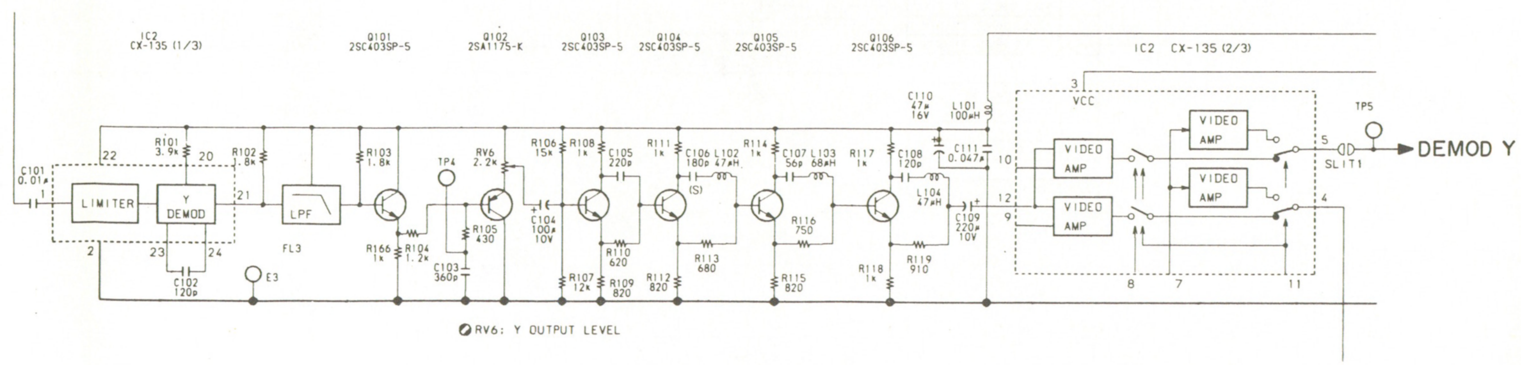


Fig. 1-4

1-1-5. Noise Canceller and Waveform Shaper Circuits

The VP-5020's video circuit has no secondary beat canceller circuit. (A secondary beat with a frequency of approximately 1.4 MHz which is double the chroma band frequency of 688 kHz appears on the screen as a beat.) The noise canceller circuit consists of two stages to prevent the occurrence of the beat.

Noise Canceller Circuit (1)

The signal fed to pin 19 of IC2 is compensated at approximately 3 MHz and video-amplified using C139, L108, and R165 at pin 17. The resultant signal passes through a high-pass filter (C113 and R122) at pins 15 and 16 of IC2 and is sent again to limiter IC2. The signal fed to limiter IC2 and the signal passed through the video amplifier are subtracted, and the resultant signal is fed to pin 14 of IC2.

Noise Canceller Circuit (2)

The signal supplied to pin 14 of IC2 passes through buffer Q107 and is amplified using Q109. In this case, the phase is inverted because it is the collector output. The amplified signal is passed through a high-pass filter (R132 and L105) and sent to limiter IC6. The limiter output is cancelled using a low-pass filter (R135, C122, and R136) at 1.4 MHz.

Waveform Shaper Circuit

The waveform shaper circuit is provided because the high-frequency waveform deteriorates due to the two-stage noise canceller circuit.

The high-frequency signal waveform from amplifier Q110 is shaped using C124. The signal from the emitter of Q111 is sliced using diodes D101 and D102 and the noise is eliminated. The high-frequency signal which passed through noise canceller circuits (1) and (2) are mixed at Q108. The resultant signal is also mixed with the chroma signal. The mixed signal is fed from Q108 and passed through a false VD insertion circuit (Q112 and Q113). It appears at an impedance of 75 ohms through an output buffer (Q114, Q115, and Q116). The 1Vp-p video signal from output buffer Q117 is sent to the RF modulator.

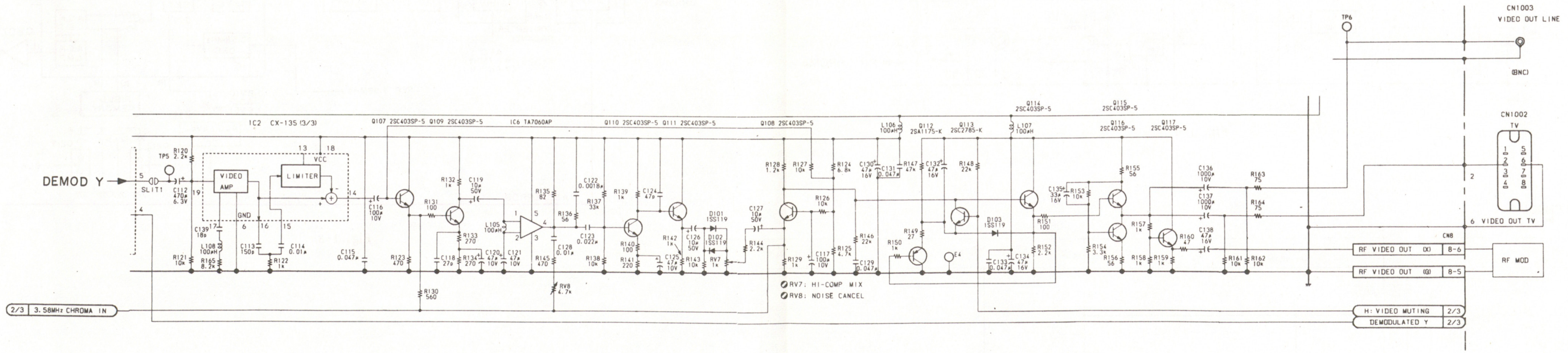


Fig. 1-5

1-1-6. Chroma System

During playback, the low-frequency chroma gain decreases because of the use of a rotary transformer, and the corresponding high-frequency chroma gain also decreases. The CH-A/B RF AMP output signal from pins 16 and 17 of IC1 is fed to a chroma frequency response compensator circuit (C201 and R201).

The chroma signal passing through the LPF and FL2 is sent to an equalizer (Q201, L202, R207, and C203) and is fed through amplifier Q202 and buffer Q203 to pin 5 of IC3 (at TP7). The signal at pin 5 is then passed through ACC amplifier IC3 to pin 3 of IC3. The carrier leakage is adjusted using RV11; the signal at pin 3 is fed to pin 2 of IC3 and sent to the frequency converter (up converter). The frequency-converted signal (688 kHz to 3.58 MHz) is fed from pin 24 of IC3 to band-pass filter FL4. Q204 mutes the chroma system in the B/W mode or when the chroma signal level is low. The output of the band-pass filter is sent from Q205 through chroma mix level control RV12 to Y/C mix circuit Q108. Q204 is a chroma muting switch.

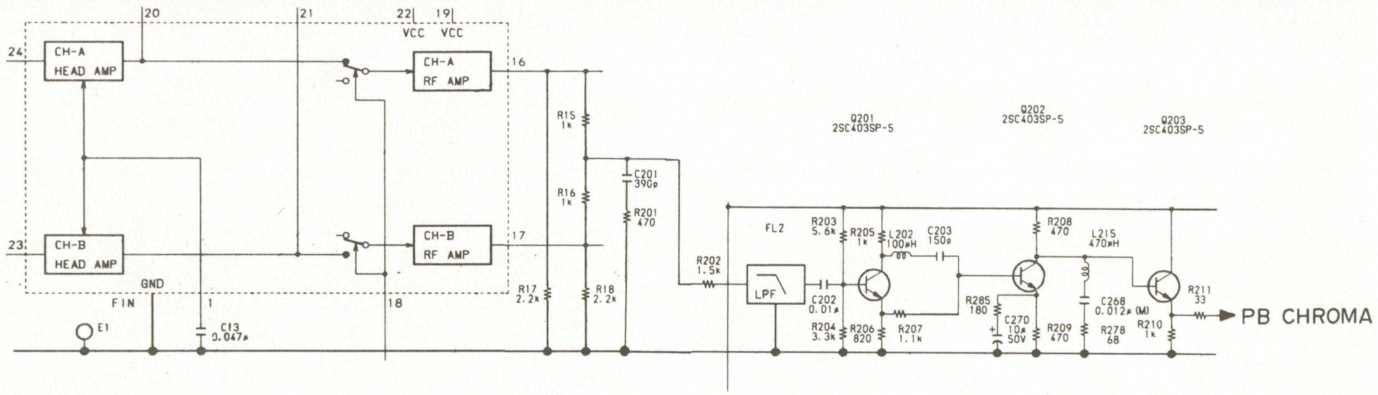


Fig. 1-6

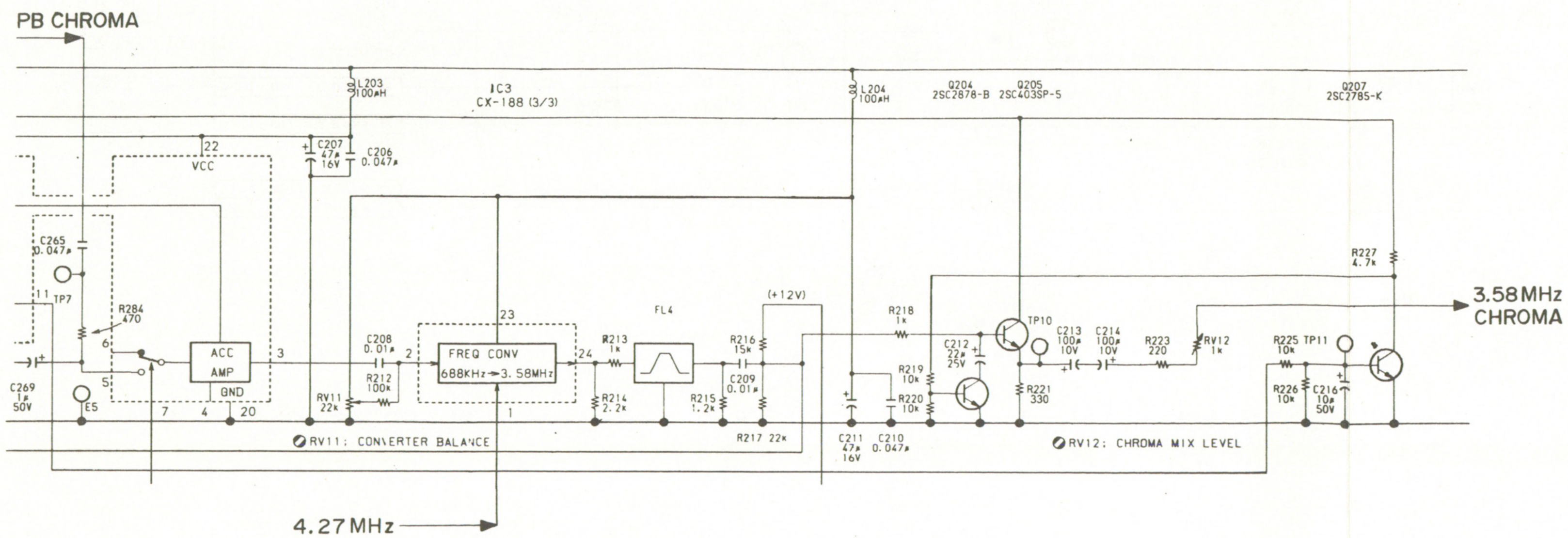


Fig. 1-7

1-1-7. ACC Circuit

The 688 kHz playback chroma signal is fed to TP7 and pin 5 of IC3. The output signal from pin 3 of IC3 passes through ACC amplifier IC3. The resultant signal is balanced using RV11 and fed to pin 2 of IC3. The resultant 4.27 MHz (± 688 kHz) chroma signal is passed through frequency converter IC3. Only a 3.58 MHz chroma signal is supplied from the band-pass filter. The 3.58 MHz chroma signal is then fed to pin 13 of IC3.

The Y video signal from pin 4 of IC2 is sent through a low-pass filter (L205 and C218) to pin 22 of IC4. The resultant signal is sync-separated in IC4, and an HD pulse is output from pin 24. The HD pulse is supplied using L211 and L212. It is fed to pin 16 of IC3 as the burst flag. The burst flag is also fed to the ACC and APC burst gates. The output signal from the burst gates is sent to an ACC detector. It is the circuit which compares the level of the signal from the burst gates with a 3.58 MHz reference input signal at pin 21 of IC3, and an error voltage appears. The error voltage changes the gain of ACC amplifier. This is the ACC loop. The ACC level is adjusted using RV10 which is located at pin 18 of IC3. The 3.58 MHz reference input signal is oscillated using X1 and CV1.

Q211 is used as a switch in the BIDIREX mode.

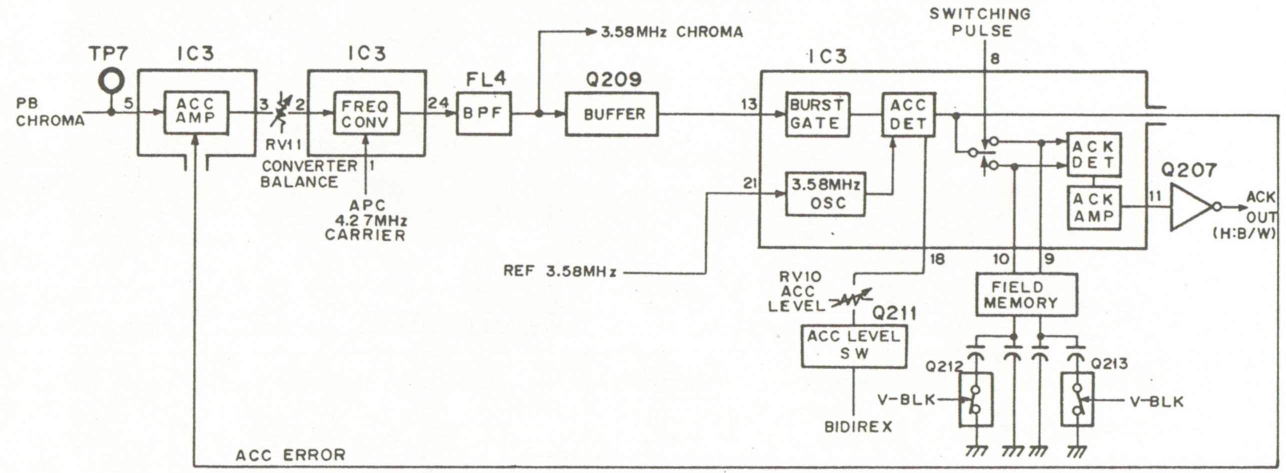


Fig. 1-8

1-1-8. ACK Circuit

A switching pulse is fed to pin 8 of IC3. ACC and ACK circuit operations are detected every field by selecting the output (ACC error voltage) of the ACC detector circuit. A field memory is provided at pins 9 and 10 of IC3. In the field memory, C260 and C262 are charged or discharged using a vertical blanking pulse to balance the DC voltage between the channels.

1-1-9. APC Circuit

The signal, which is burst gated using the burst gate flag as in the ACC circuit, is fed to the APC detector circuit. The APC detector circuit compares the input burst gated signal phase with the phase of a 3.58 MHz reference signal. The error is sent as a DC voltage to pin 14 of IC4.

In the NTSC model, a burst tuning amplifier is not used, but a continuous 4.43 MHz signal from the reference oscillator is fed to pin 21 of IC3. It is compared with the input from pin 13.

Detector and canceller circuits are provided in the APC loop in case the fH frequency on the tape is delayed or advanced and the APC loop is false-locked. These circuits change the VCO frequency by adding an APC ID signal to the APC error voltage.

The Y signal fed from pin 4 of IC2 to R228 passes through a low-pass filter (L205 and C218) to pin 22 of IC4. The signal at pin 22 is then passed through sync separator and half H killer circuits in the IC and is frequency-divided by eight. The resultant signal is used to reset the counter. The 1/8-frequency-divided signal is compared using an internal digital comparator at all times. An ID signal is then produced, and the VCO frequency is raised or lowered to control the APC loop lock in the normal range.

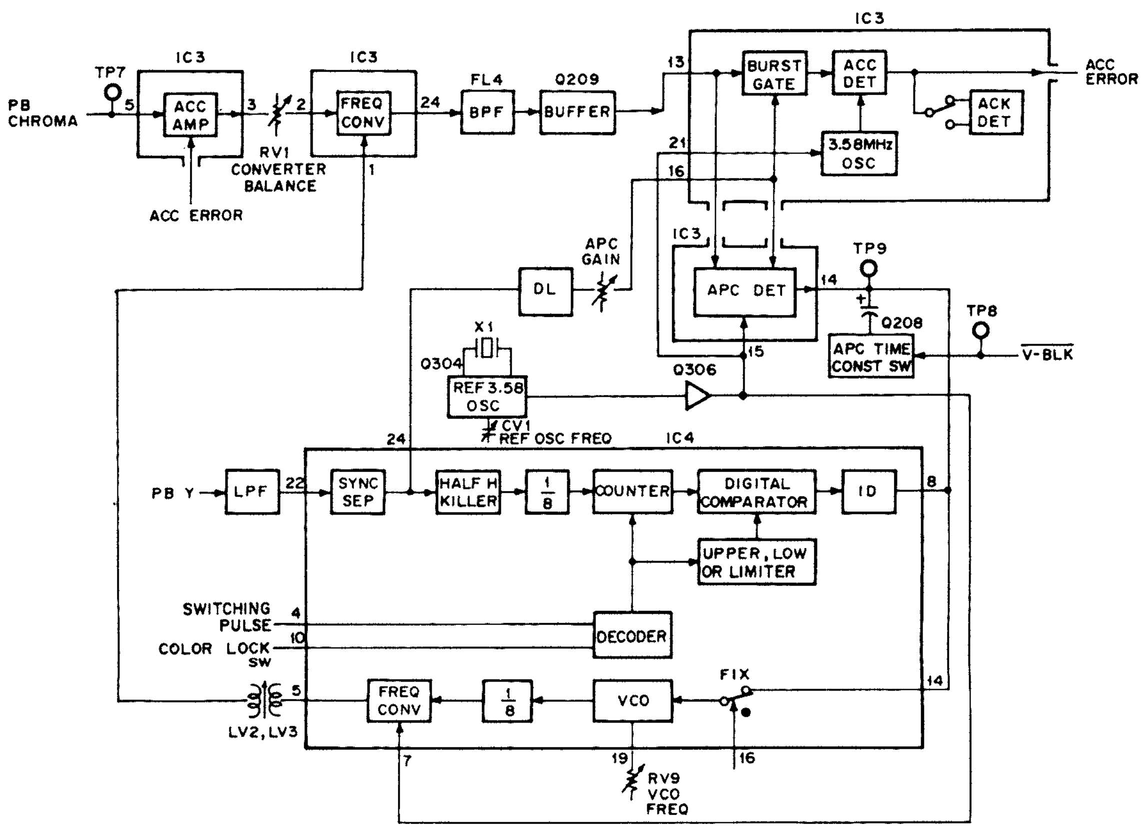


Fig. 1-9

1-1-10. False VD Circuit

A vertical blanking pulse is sent to pins 1 and 2 of IC7 to produce a false VD (vertical drive) pulse. The resultant pulse is then passed through amplifier Q307 and fed to insertion circuit Q103.

The vertical blanking pulse is also fed to pin 6 of IC7 as an output control signal in the BIDIREX mode. Q303 is a 9V REG power supply for the RF unit.

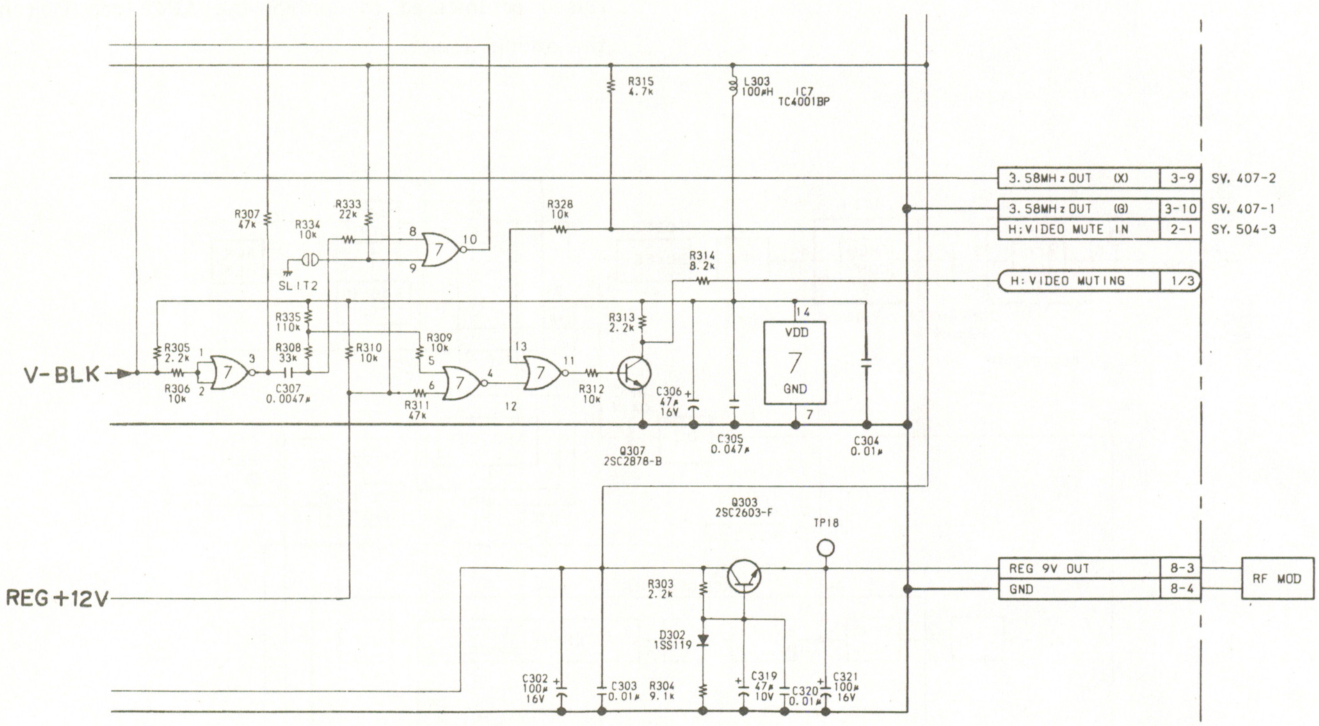


Fig. 1-10

1-2. FOR VP-5040

1-2-1. RF Amplifier

The RF signal from the video head passes through the input transformer (T1 and T2),and is amplified by FETs Q1 and Q2 whose S/N ratio is excellent. The resultant signal is fed to pins 23 and 24 of IC1 (CX134A). It is then sent through the head amplifier and RF amplifier to pins 16 and 17.

The CH-A and CH-B RF output signals are compensated in the middle range of their frequency response by capacitors and coils connected to pins 20 and 21. They are supplied from pins 16 and 17 of IC1.

Channel A is described below. This circuit contains a negative feedback loop between R7 and Q1. This feeds back the voltage from a voltage divider (R7 and R8). The peak value of the frequency response should reach 6 to 7 MHz, it is detected using an LC circuit (C7 and L2). If an unbalanced frequency response is caused by deviations between the heads for channels A and B, it can be adjusted using RV1. The RF output signal from pins 16 and 17 of IC1 is balanced using RV3. The resultant RF signal level is adjusted using RV4. The signal passes through buffer Q4. The RF signal from Q4 passes through TP1 and high-pass filter FL1. The resultant Y RF signal is then sent to pin 14 of IC1.

Pin 15 of IC1 selects black and white. For the VP-5040, however, the color mode is fixed with pin 12 connected to ground.

The Y RF signal passes through a Y RF amplifier and limiter in IC1. It is then passed through a dropout compensation switch. The RF signal with no dropout is fed from pin 4 of IC1 to Q5.

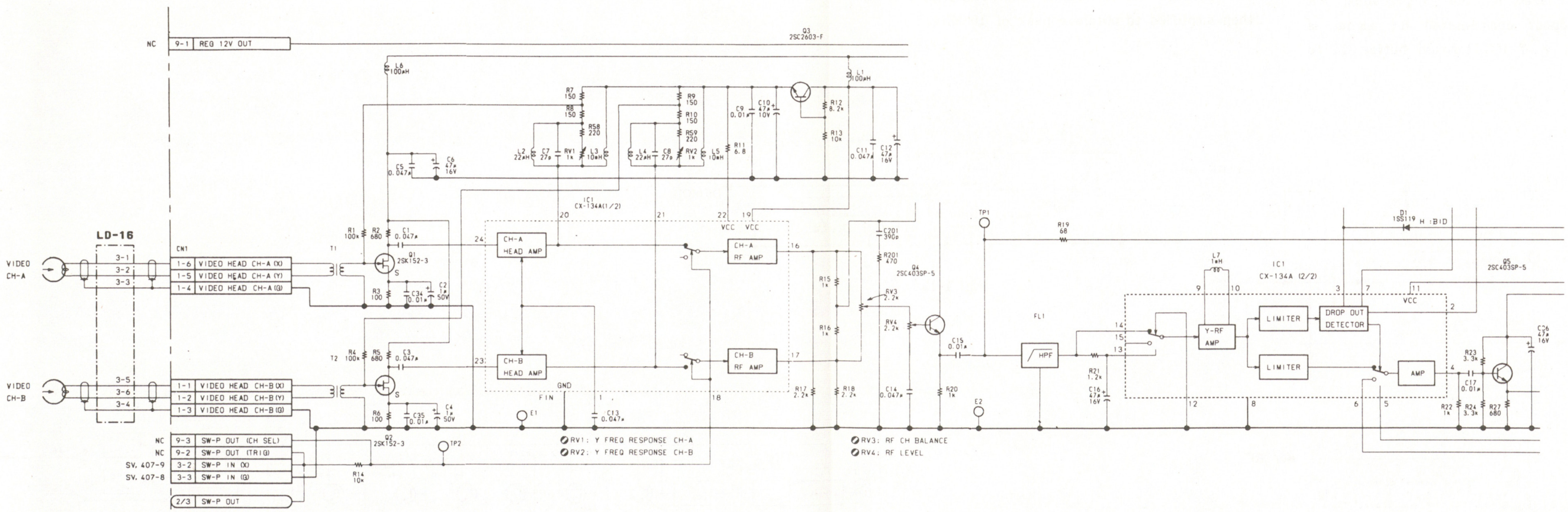


Fig. 1-11

1-2-2. Dropout Compensation Circuit

This is the circuit that inserts the 1H-preceding RF signal into the dropout portion of the RF signal. Dropout is detected using an RF signal envelope detector circuit consisting of C21 and R45. Sensitivity is adjusted by changing the bias voltage of this circuit. The dropout detection sensitivity is determined by the input level at pin 14 of IC1 and adjusted using RV5. A dropout pulse from pin 2 of IC1 turns on Q7, which provides hysteresis for the detection level. Muting switch of dropout detector D1 is used to mute the dropout in the search mode.

The 1H-delayed signal is fed to pin 6 of IC1. The RF signal from buffer Q5 is 1H-delayed using delay line DL2. When dropout is detected in IC1, the dropout compensation switch is set to the DROPOUT position. This enables the dropout portion to be replaced by the 1H-preceding RF signal. The dropout compensated RF signal is supplied from pin 4 of IC1 through buffer Q5 to pin 9 of IC5.

1-2-3. PB, Y RF Sideband Equalizer

Durinf playback of a magnetic recording, demodulation often occurs, because the high-frequency level attenuates.

When the high-frequency RF signal level is low, the high-frequency signal cannot be properly demodulated completely, but is demodulated as a low-frequency signal. Black stripes appear on the monitor screen. Therefore, the high-frequency signal level is raised to prevent overmodulation.

The dropout compensated RF signal passes through limiter IC5 (1/3) and is sent from pin 6 of IC5. One of the resultant outputs passes through R32 and R33 and is sent to differential amplifier IC5 (2/3). The other output is fed through delay line DL1 to pin 4 of IC5. When the RF signal level is lowered, the signal at pin 4 is high-frequency boosted using differential amplifier IC5 because of its cosine characteristic. It is then amplified to obtain a peak of 10 MHz.

1-2-4. Demodulator

The RF signal at pin 2 of IC5 is fed to pin 1 of IC2 and demodulated through a limiter. The demodulated signal is appears at pin 21. The capacitor between pins 23 and 24 of IC2 determines the linearity of the demodulated signal. The output at pin 21 passes through low-pass filter FL3 and becomes a demodulated video signal with the impedance of R102. The demodulated video signal passes through buffer Q101, and a deemphasis circuit (R104, R105, and C103).

The video level is adjusted using RV6 which is located at the emitter of Q102 so that the level at TP6 is 1Vp-p when the VIDEO OUT connector is terminated in 75 ohms. The output of the deemphasis circuit is fed through an equalizer consisting of Q103 through Q105 to buffer Q106 and input to pin 12 of IC2 at approximately 250mVp-p. The resultant signal passes through video amplifier IC2, then is output to pin 5 of IC2 at approximately 1Vp-p and to pin 4 of IC2 at approximately 2Vp-p.

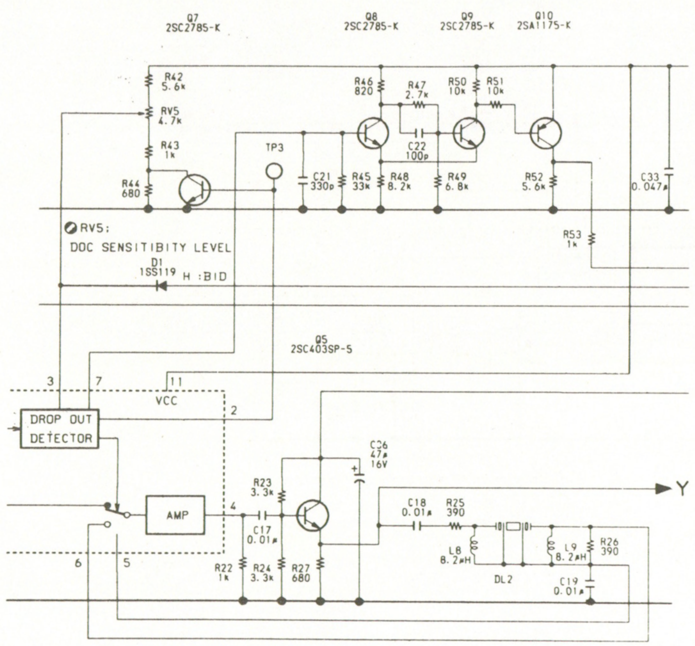


Fig. 1-12

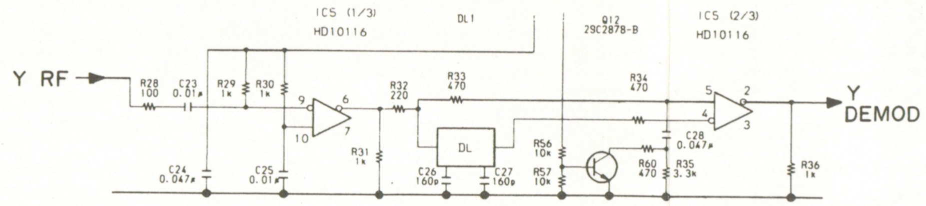


Fig. 1-13

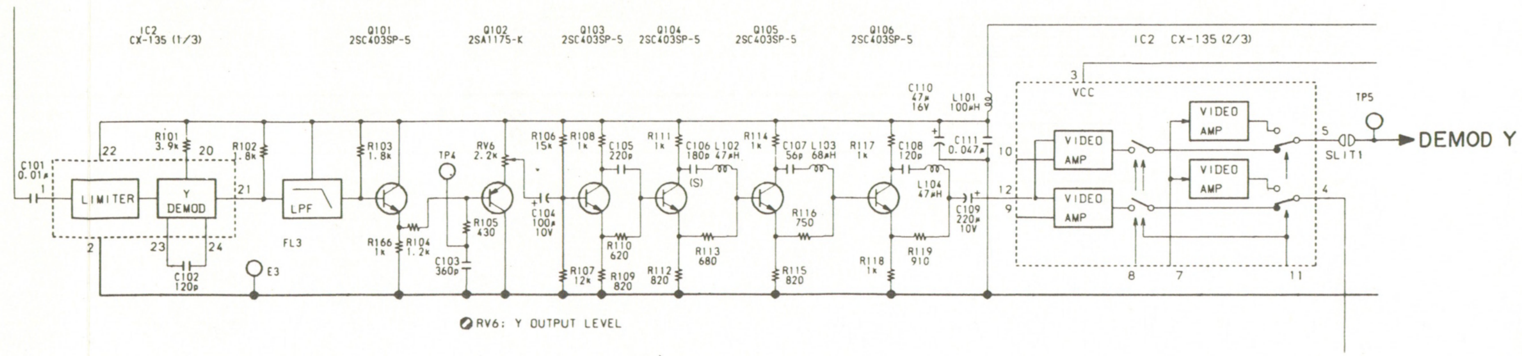


Fig. 1-14

1-2-5. Noise Canceller and Waveform Shaper Circuits

The VP-5040's video circuit has no secondary beat canceller circuit. (A secondary beat with a frequency of approximately 1.4 MHz which is double the chroma band frequency of 685 kHz appears on the screen as a beat.) The noise canceller circuit consists of two stages to prevent the beat.

Noise Canceller Circuit (1)

The signal fed to pin 19 of IC2 is compensated at approximately 3MHz and video-amplified using C139, L108, and R165 at pin 17. The resultant signal passes through a high-pass filter (C113 and R122) at pins 15 and 16 of IC2 and is sent again to limiter IC2. The signal fed to limiter IC2 and the signal passed through video amplifier are subtracted, and the resultant signal is fed to pin 14 of IC2.

Noise Canceller Circuit (2)

The signal output to pin 14 of IC2 passes through buffer Q107 and is amplified using Q109. In this case, the phase is inverted because of its collector output. The amplified signal passes through a high-pass filter (R132 and L105) and is sent to limiter IC6. The limiter output is cancelled using a low-pass filter consisting of R135, C122, and R136 at 1.4MHz.

Waveform Shaper Circuit

The waveform shaper circuit is provided because the high-frequency waveform deteriorates due to the two-stage noise canceller circuit. The signal from amplifier Q110 is shaped using C124. It is then sliced using the emitter of Q111 and diodes D101 and D102 and the noise is eliminated. The high-frequency signal passing through C127 and RV8 and the signal passing through noise canceller circuits (1) and (2) are mixed using Q108. The resultant signal is also mixed with the chroma signal. The output of Q108 passes through a false VD insertion circuit (Q112 and Q113) and at an impedance of 75 ohms is sent through an output buffer (Q114 through Q116). The 1Vp-p video signal from output buffer Q117 is sent to the RF modulator.

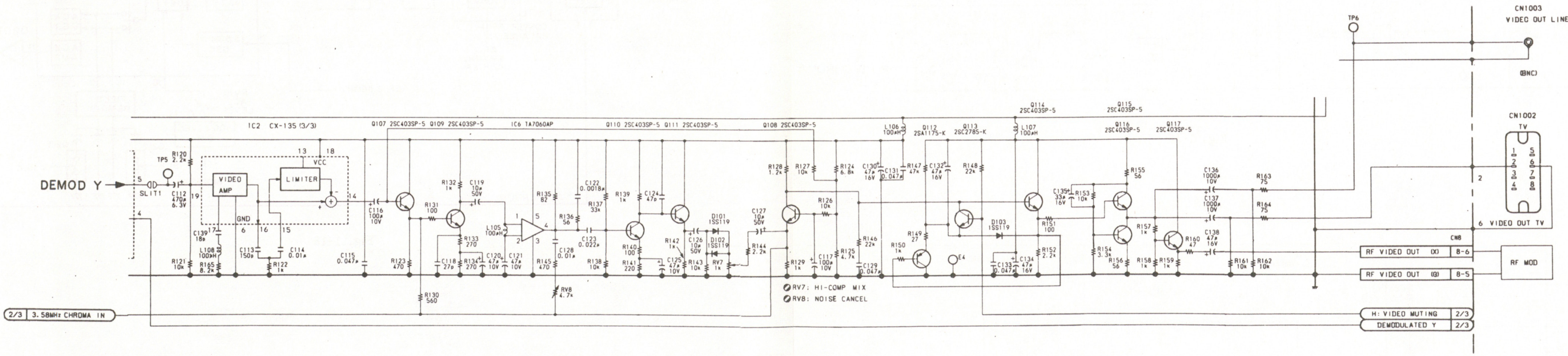


Fig. 1-15

1-2-6. Chroma System

The CH-A/B RF AMP output signal from pins 16 and 17 of IC1 is fed to a chroma frequency response compensator circuit (C201 and R201. At that time, the low-frequency chroma gain decreases through a rotary transformer, so that the corresponding high-frequency chroma gain also decreases.

The chroma signal passing through the LPF and FL2 is sent to an equalizer (FQ201, L202, R207, and C203) and is fed through amplifier Q202 and buffer Q203 to pin 5 of IC3 (at TP7). The signal at pin 5 is then passes through ACC amplifier IC3 to pin 3 of IC3. The carrier leakage is adjusted using RV11 and the signal at pin 3 is input to 2 of IC3. The playback chroma signal is sent from pin 2 of IC3 to the frequency converter (up converter). The frequency-converted chroma signal (685 kHz to 4.43 MHz) is fed from pin 24 of IC3 to band-pass filter FL4. Q204 mutes the chroma system in the B/W mode or when the chroma signal level is low. The output of band-pass filter FL4 is sent from Q205 through chroma mix level control RV12 to Y/C mix circuit Q108. Q206 turns on when a SECAM signal is fed and eliminates a change in chroma level, which is caused by the level difference between the PAL and SECAM burst signals.

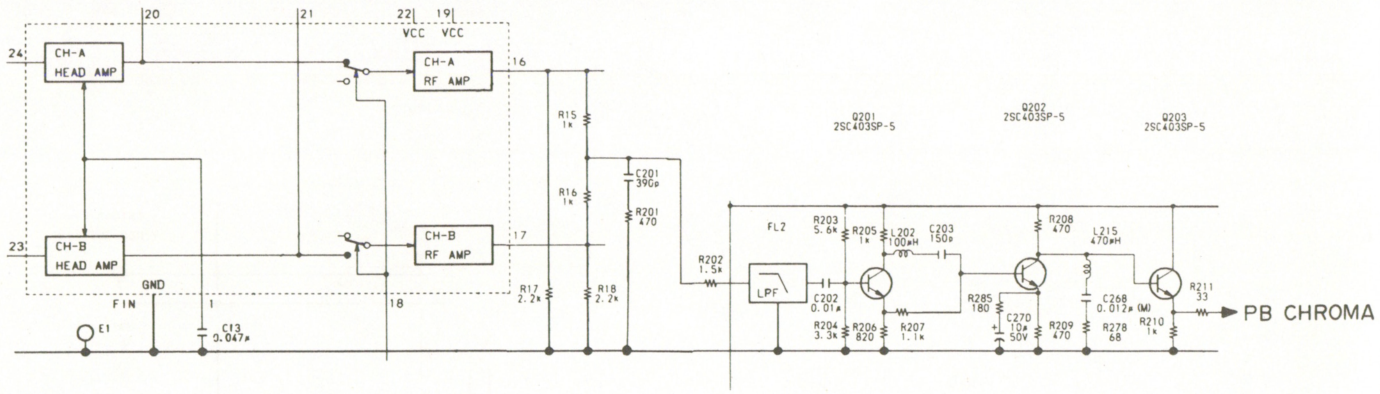


Fig. 1-16

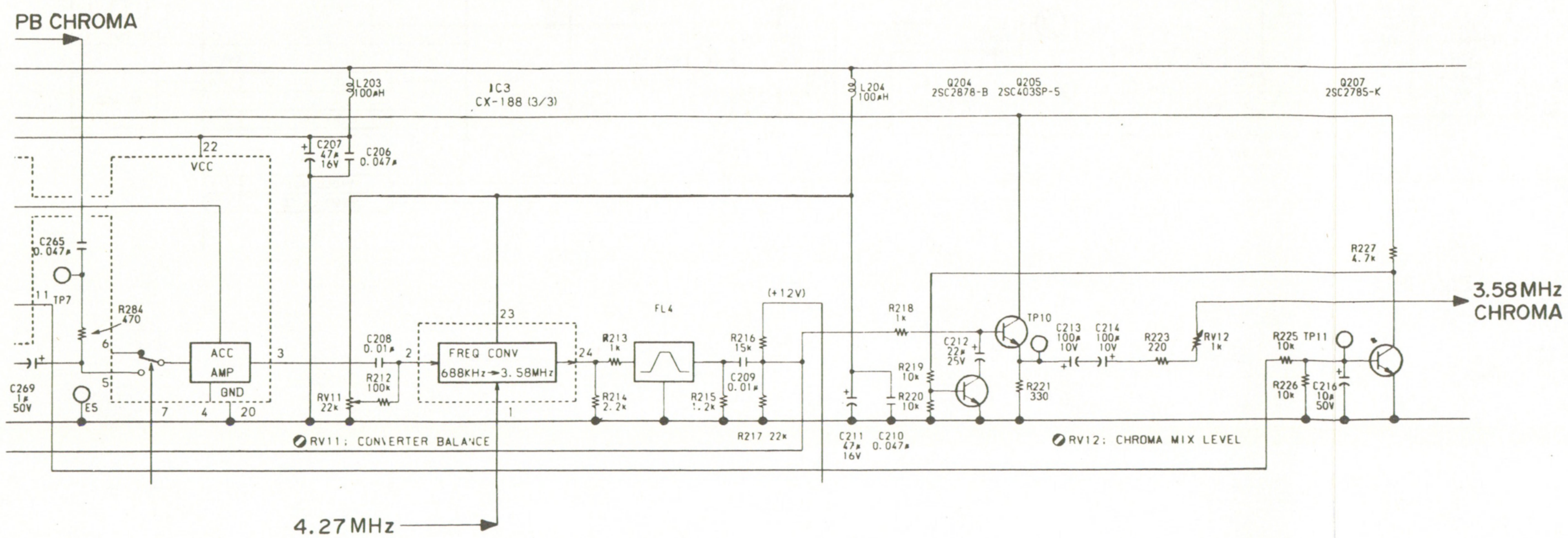


Fig. 1-17

1-2-7. ACC Circuit

The 685 kHz playback chroma signal is fed to TP7 and pin 5 of IC3. The chroma output signal from pin 3 of IC3 is passed through ACC amplifier IC3. It is converter-balanced using RV11, then input to pin 2 of IC3. The resultant signal passes through frequency converter IC3 to become the 5.12 MHz (± 685 kHz) chroma signal. Only a 4.43 MHz chroma signal is supplied from the band-pass filter. The 4.43 MHz chroma signal then passes through buffer Q209. It is fed from a burst amplifier (Q210 and LV1) to pin 13 of IC3.

The Y video output signal from pin 4 of IC2 is fed through a low-pass filter (L205 and C218) to pin 22 of IC4. The resultant signal is sync-separated in IC4, and an HD pulse is supplied from pin 24. The HD pulse is delayed using L211 and L212 and fed to pin 16 of IC3 as a burst flag. The burst flag is sent to the ACC and APC burst gates. In the ACC loop, the output singal from the burst gates is sent to an ACC detector circuit. In the circuit, the level of the signal from the burst gates is compared with a 4.43 MHz reference input signal at pin 21 of IC3. In this way, an error voltage is obtained. The error voltage changes the gain of ACC amplifier. This is the ACC loop. The ACC level is adjusted using RV10 whch is located at pin 18 of IC3. Q211 is used as a switch in the BIDIREX mode. The 4.43 MHz reference input signal is oscillated using X1 and CV1.

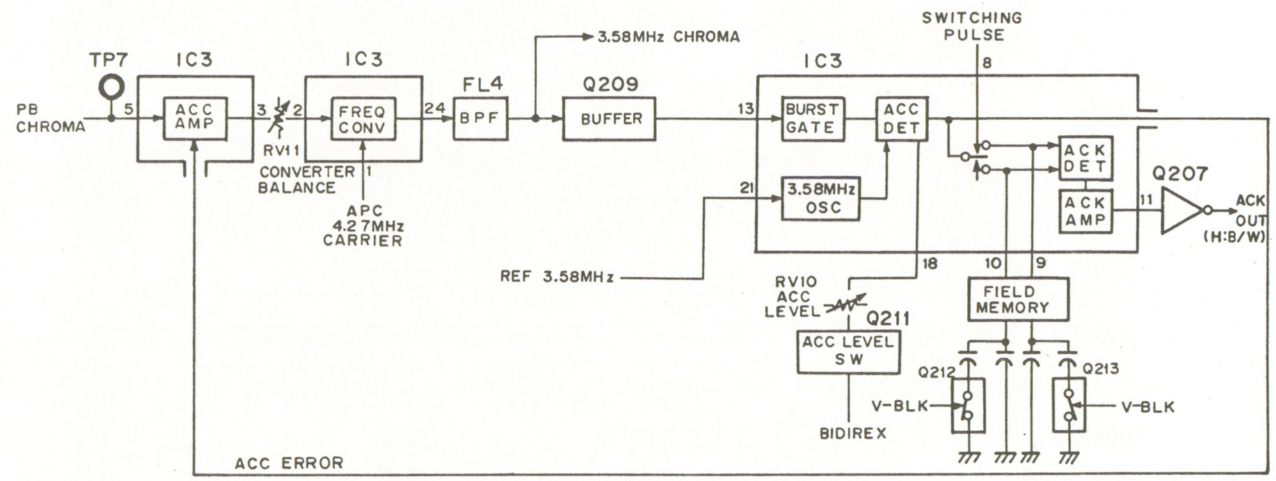


Fig. 1-18

1-2-8. ACK Circuit

A switching pulse is fed to pin 8 of IC3. ACC and ACK circuit operations are detected every field by selecting the output (ACC error voltage) of the ACC detector circuit. A field memory is provided at pins 9 and 10 of IC3. In the field memory, C260 and C262 are charged or discharged using a vertical blanking pulse to balance the DC voltage between the channels.

1-2-9. APC Circuit

The signal, which is burst gated using the burst gate flag as in the ACC circuit, is fed to the APC detector circuit. The APC detector circuit compares the burst gated signal phase with the phase of a 4.43 MHz reference signal. The error is sent as a DC voltage to pin 14 of IC4. The VCO in IC4 is controlled using the DC voltage. The VCO oscillating frequency is counted down to 1/8 and converted into 5.12 MHz using a frequency converter. The 5.12 MHz output from pin 5 of IC4 is tuned using LV2 and LV3 and sent to pin 1 of IC3. A 685 kHz chroma signal is up-converted into 4.43 MHz using frequency converter IC3. This is the APC loop. Detector and canceller circuits are provided in the APC loop if the fH frequency on the tape is delayed or advanced and the APC loop is false-locked. These circuits change the VCO frequency by adding an APC ID signal to the APC error voltage.

The Y signal fed from pin 4 of IC2 to R228 passes through a low-pass filter (consisting of L205 and C218) to pin 22 of IC4. The signal at pin 22 then passes through sync separator and half H killer circuits in the IC and is frequency-divided by eight. The resultant signal is used to reset a counter. The 1/8-frequency-divided signal is compared using an internal digital comparator. An ID signal is then produced, and the VCO frequency is raised or lowered to control the APC loop lock in the normal range.

In the PAL system, the control range of the APC loop lock can be changed. The center frequency of the decoder in the IC is changed according to the level at pin 10 of IC4, that is H, L, or OPEN, using a color lock switch. This changes the output of the digital comparator and controls the VCO frequency.

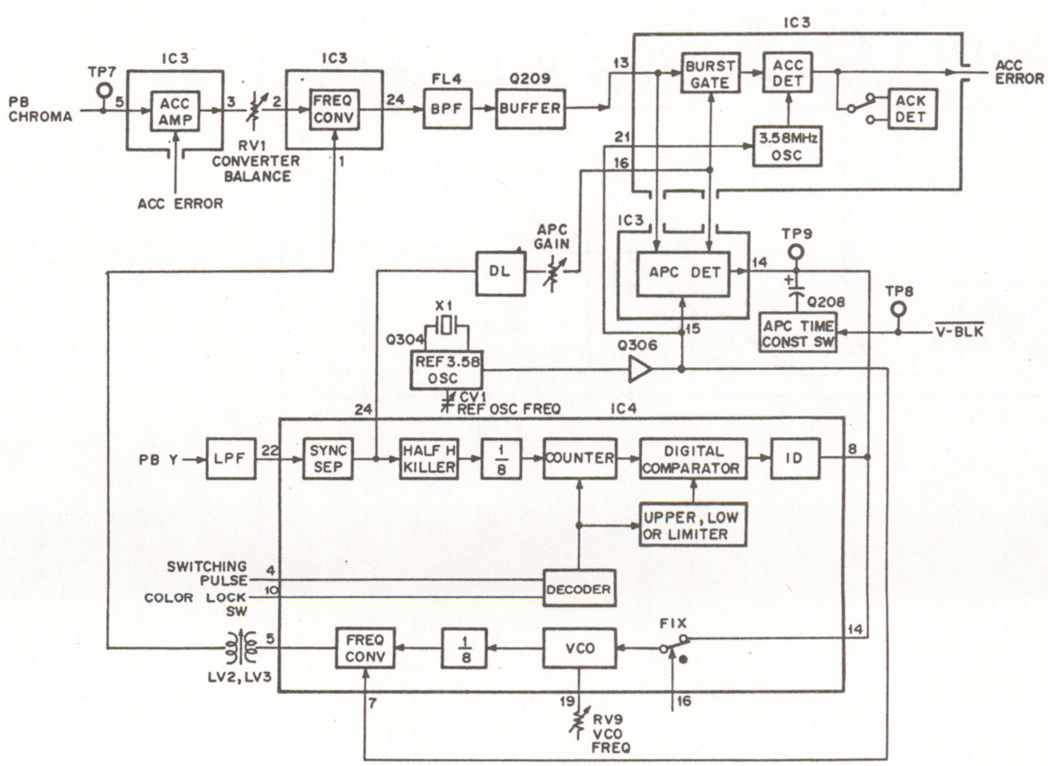


Fig. 1-19

1-2-10. False VD Circuit

A vertical blanking pulse is sent to pins 1 and 2 of IC7 to produce a false vertical drive (VD) pulse. The resultant signal then passes through amplifier Q307 and is fed to insertion circuit Q113. The vertical blanking pulse is also fed to pin 6 of IC7 as an output control signal in the BIDIREX mode.

Q303 is a 9V REG power supply for the RF unit. Q301 and Q302 are used as a detector circuit for overcurrent. When overcurrent flows and the voltage at the collector of Q302 decreases, D301 and Q301 are turned on. When Q301 is turned on, Q302 is turned off, and then REG 12V and REG 9V are turned off.

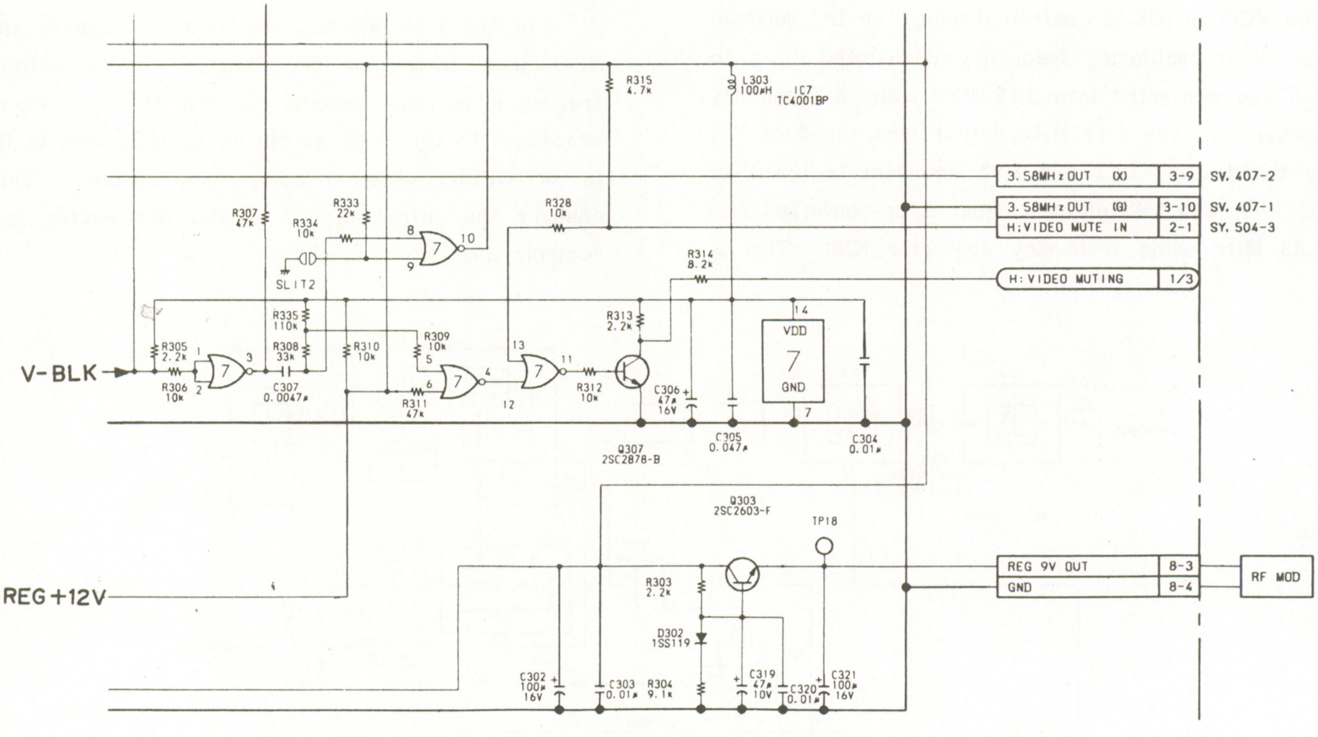


Fig. 1-20

SECTION 2
AUDIO CIRCUIT

The audio circuit on the VA-35 Board consists of a head amplifier, a line amplifier, and a muting circuit. Channels 1 and 2 are configured identically; therefore, only Channel 1 is described here. The input from the audio head is fed to pin 1 of IC901 and amplified. RV901, R907, and C909 form a head amplifier equalizer. The input (approximately -65dB) from the audio head is amplified by IC901 (to approximately -35dB, at pin 3). The resultant signal is fed from line amplifier IC902 to AUDIO MONITOR OUT and LINE OUT connectors, after the level is adjusted at RV903.

Q901 is a muting switch. The signal from the AUDIO MONITOR OUT connector is selected as CH-1, CH-2, or MIX using a switch on the KY Board, and the selected signal is sent to Q952. The signal is then fed from the emitter of Q952 as the AUDIO TV OUT, the AUDIO RF OUT, and the AUDIO MONITOR OUT (mini jack) signals.

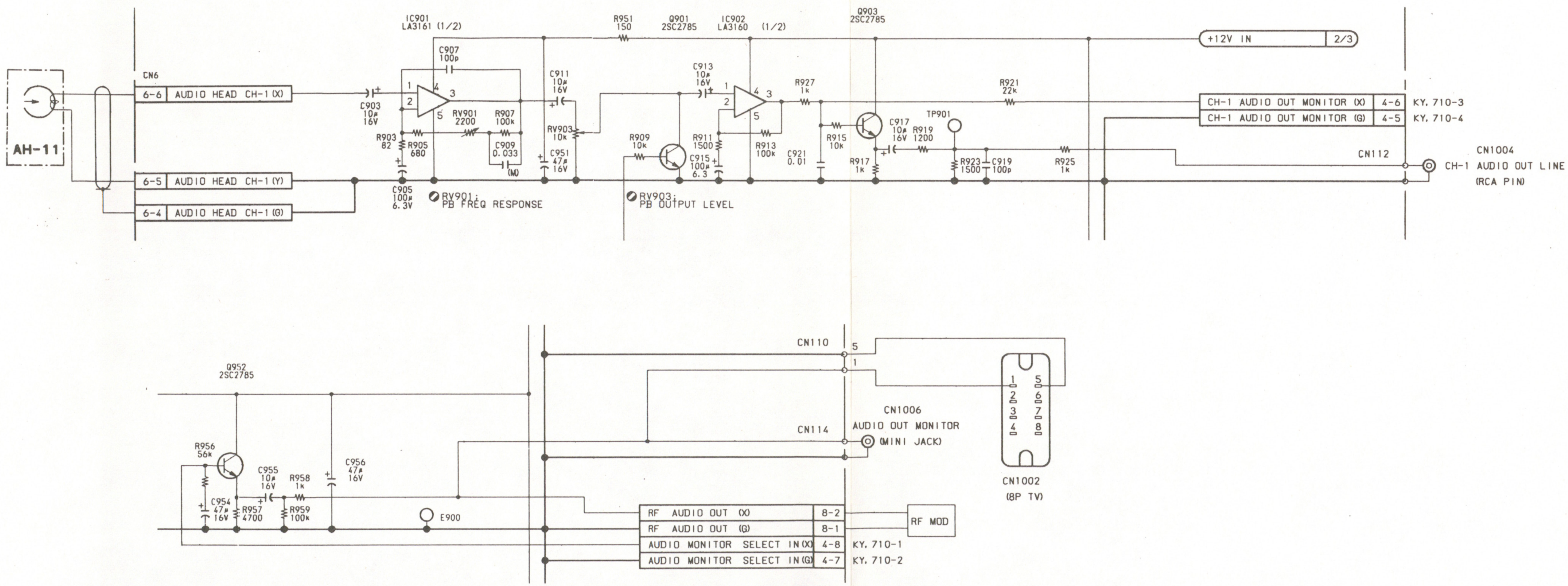


Fig. 2-1

SECTION 3
SERVO CIRCUIT

3-1. DRUM SPEED SERVO

The drum speed servo maintains a constant. difference by measuring the time difference between the SPEED PG-A pulse which is generated by drum rotation, and the SPEED PG-B pulse, whose rotation phase is delayed by it.

op The SPEED PG-A and PG-B pulses from pins 6 and 4 of connector CN10 are fed to pins 32 and 33 of IC17. The SPEED PG-A pulse is waveform-shaped using a Schmitt trigger circuit in IC17. It becomes a trigger to start the high-speed monostable multivibrator. The resultant pulse is delayed by the time constant of the RC circuit which is connected to pin 31 of IC17. The output of the monostable multivibrator is fed to set the R-S flip-flop position. The SPEED PG-B pulse is also fed through the Schmitt trigger circuit and resets the R-S flip-flop position. The R-S flip-flop feeds the pulse with a width corresponding to the drum rotation speed. The resultant pulse is then ANDed with a 2Fsc signal and converted into a pulse train of 2Fsc. The pulse train is pulse-counted using a speed detection counter. The speed data fed to a PWM (pulse-width modulator) is pulse-width modulated and sent from pin 34 of IC17.

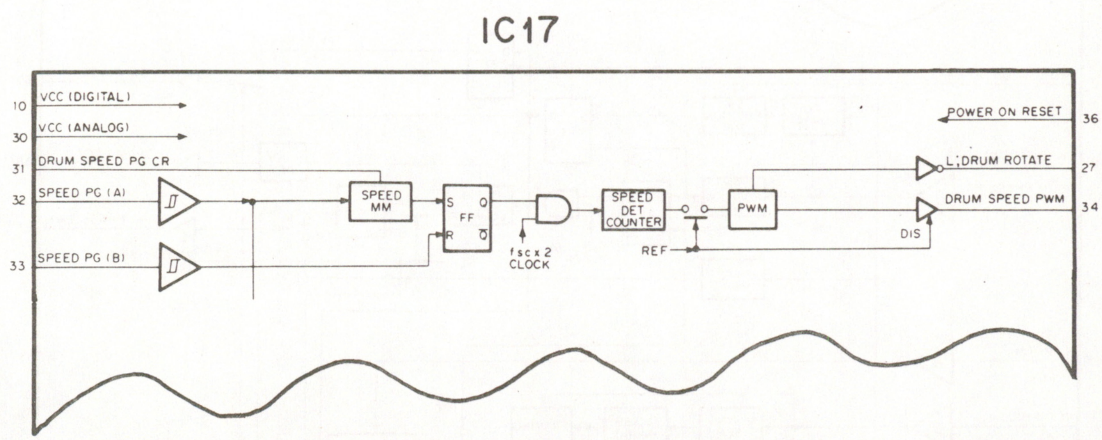


Fig. 3-1

3-2. DRUM PHASE SERVO

The drum rotation phase is controlled to make constant. The phase relation between the PHASE PG pulse and the 1/2 VD pulse generated from a reference sync signal. The PHASE PG pulse from pin 2 of connector CN10 is fed to pin 40 of IC17.

The PHASE PG pulse is waveform-shaped using a Schmitt trigger circuit to start the trigger SW position of the monostable multivibrator. The resultant pulse is delayed by the time constant which is connected to pin 41 of IC17. The output of the monostable multivibrator is supplied to set the R-S flip-flop. The 1/2 VD pulse generated from the reference sync signal, which is sent to pin 3 of IC17, is fed to reset the R-S flip-flop. A pulse with a width corresponding to the phase is sent from the R-S flip-flop. The pulse is then ANDed with a 1/4Fsc signal and converted into a pulse train of 1/4Fsc. The pulse train is pulse-counted using a phase detection counter. A pulse with a width proportional to the data, is supplied from pin 37 of IC17 as the pulse-width modulated pulse.

3-3. VIDEO HEAD SWITCHING

The PHASE PG pulse fed to pin 40 of IC17 is delayed to switching position A by the time constant of the RC circuit, which is connected to pin 41 of IC17. The pulse is also sent to the reset input of a switching pulse flip-flop.

The SPEED PG-A pulse fed to pin 32 of IC17 is passed through a PG gate (4-bit shift register). The resultant output is delayed to switching position B by the time constant of the RC circuit which is connected to pin 2 of IC17. The pulse is also sent to set the switching pulse flip-flop.

The output of the R-S flip-flop is passed through a D-T flip-flop and locked to the H sync signal. The output at pin 39 of IC3 becomes a H sync-locked RF switching pulse when a sync signal exists.

IC17

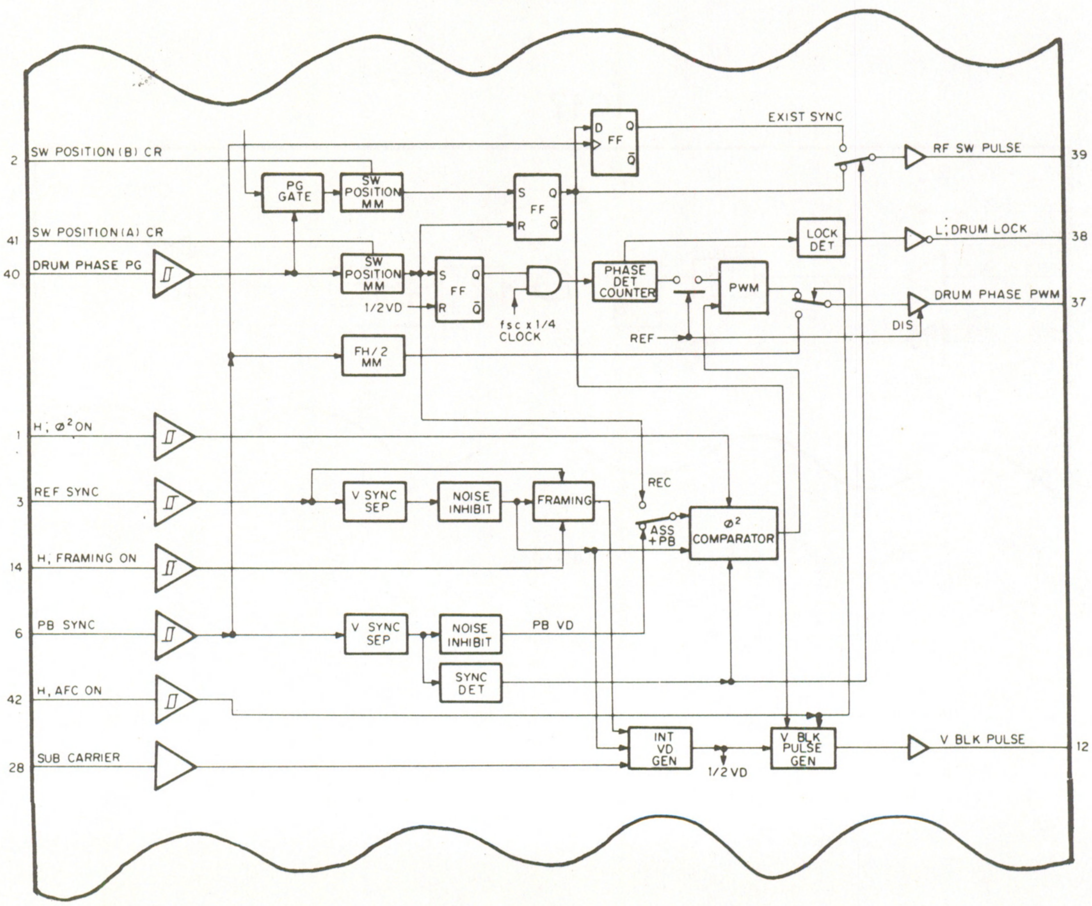


Fig. 3-2

3-4. DRUM MOTOR DRIVER

In the NORMAL mode, the drum phase PWM (pulse-width modulated) pulse is fed from pin 37 of IC17. It is also passed through a low-pass filter (R7, C3, and C4) and converted into a DC voltage. The DC voltage is sent through limiter IC1 and switch IC5 to pin 9 of IC1.

In the SEARCH mode, the line frequency for the playback picture appears at pin 37 of IC17 instead of the drum phase PWM. The resultant output is passed through switch IC5 and a low-pass filter (C10 and C11). It is amplified using IC1, and sliced using D3 and D5. The sliced output is sent through buffer IC1 and switch IC5 to pin 9 of IC1.

The DC voltage is previously set using RV1 so that no transient occurs when the mode is switched from NORMAL to SEARCH.

When the signal level at pin 42 of IC17 changes from low to high, AFC select (NORMAL/SEARCH) switch IC5 is delayed using C9, R22, and R21. The drum speed PWM is converted into a DC voltage using low-pass filter IC17. The DC voltage is sent to pin 10 of IC1. The difference between the inputs at pins 9 and 10 of IC1 is sent from pin 8 of IC1. The output at pin 8 is amplified using Q3, Q4, and Q5 and fed to the motor.

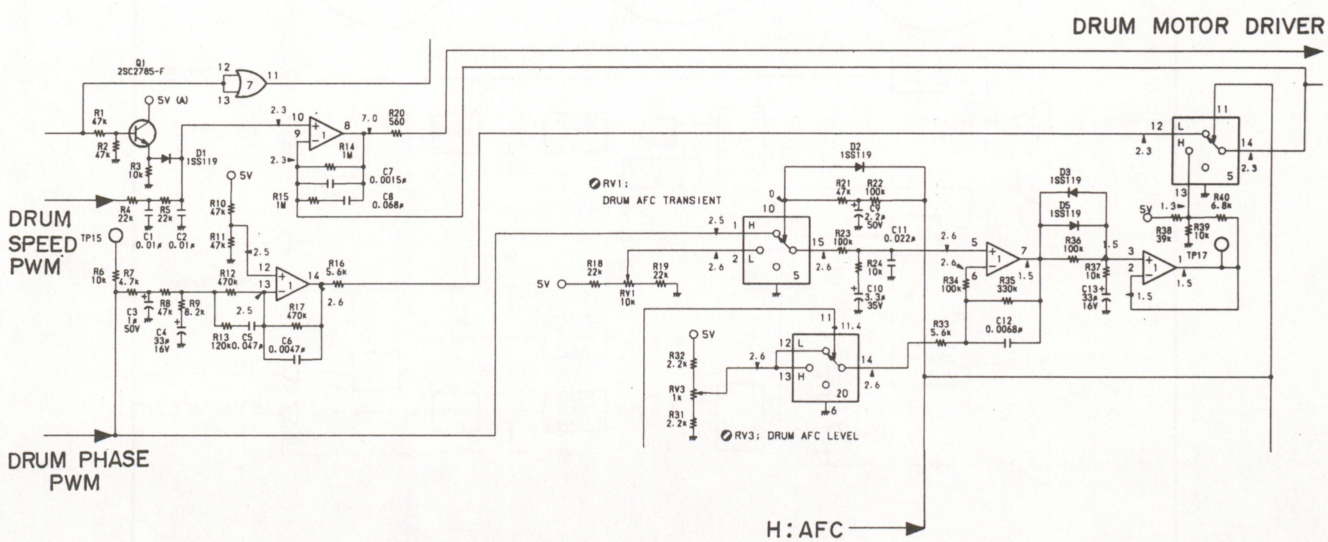


Fig. 3-3

3-5. CAPSTAN SPEED SERVO

The capstan speed servo maintains a constant time difference between the FG (A) and FG (B) pulses on the coaxial shaft of a capstan motor.

The FG (A) and FG (B) pulses fed to pins 17 and 18 of IC17 are passed through a Schmitt trigger circuit and supplied to set and reset the R-S flip-flop. A pulse with a width corresponding to the time difference between the FG (A) and FG (B) pulses appears at the output of the flip-flop. The resultant pulse is ANDed with a 1/2 Fsc and converted into a pulse train of 1/2 Fsc. The pulse train is pulse-counted using a speed detection counter. A pulse proportional to the data appears at pin 24 of IC17.

3-6. CAPSTAN PHASE SERVO

The capstan phase servo maintains a constant relation between the PB CTL signal and the 1/2 VD pulse generated in the IC.

The 1/2 VD pulse is delayed using a tracking MMV (monostable multivibrator) and supplied to set the R-S flip-flop. The PB CTL passing through pin 16 of IC17 is fed to reset. A pulse with a width corresponding to the time difference between the 1/2 VD pulse and PB CTL signal appears at the output of the flip-flop. A pulse-width modulated pulse proportional to the data, is sent from pin 20 of IC17.

IC17

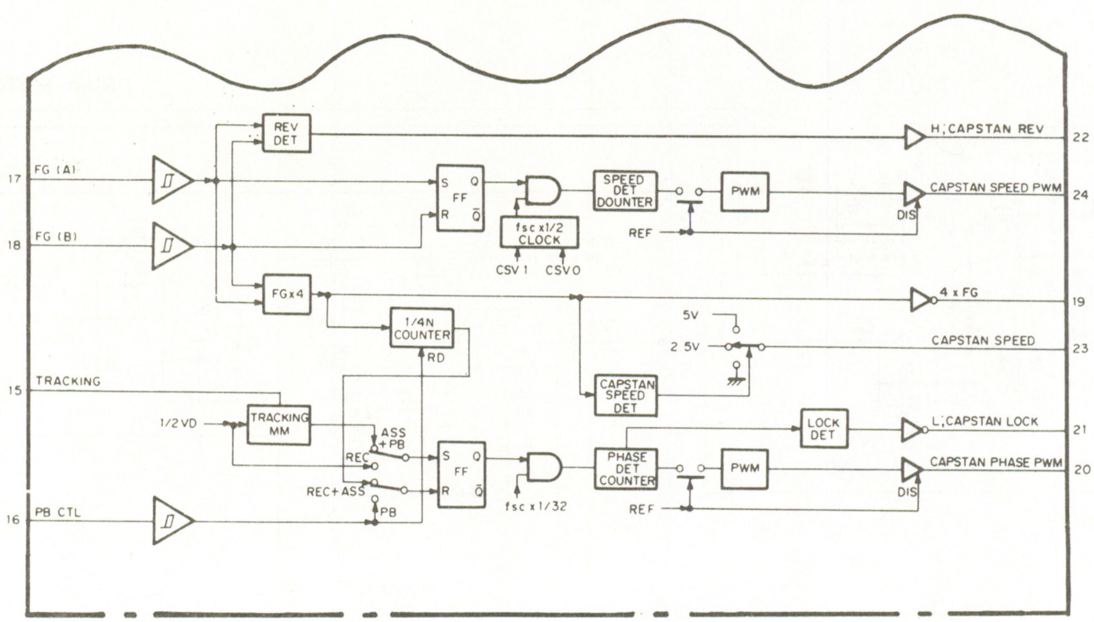


Fig. 3-4

3-7. CAPSTAN MOTOR DRIVER

In the NORMAL PB mode

The capstan speed PWM pulse at pin 24 of IC17 is passed through a low-pass filter (R157, R158, C114, and C115). It is then sent to pin 3 of differential amplifier IC8. (When the capstan is changed from the STOP mode to the PLAY mode, the signal at pin 3 of IC8 remains high by passing through Q110 and D106 from pin 23 of IC17, until the capstan speed exceeds 1/10 the normal speed.)

The capstan phase PWM (pulse-width modulated) at pin 20 of IC17 is passed through a low-pass filter (IC12 and IC8) and sent to the comparator at pin 6 of IC8 as a DC voltage. This DC voltage is compared in this comparator with the DC voltage (capstan free speed) adjusted at RV100. The DC voltage difference is sent from pin 7 of IC8. The resultant output is fed to pin 2 of IC8. The difference between the capstan speed PWM fed to pin 3 of IC8 and the DC voltage is sent from pin 1. The output is amplified using Q111 and Q112 and sent to the capstan motor.

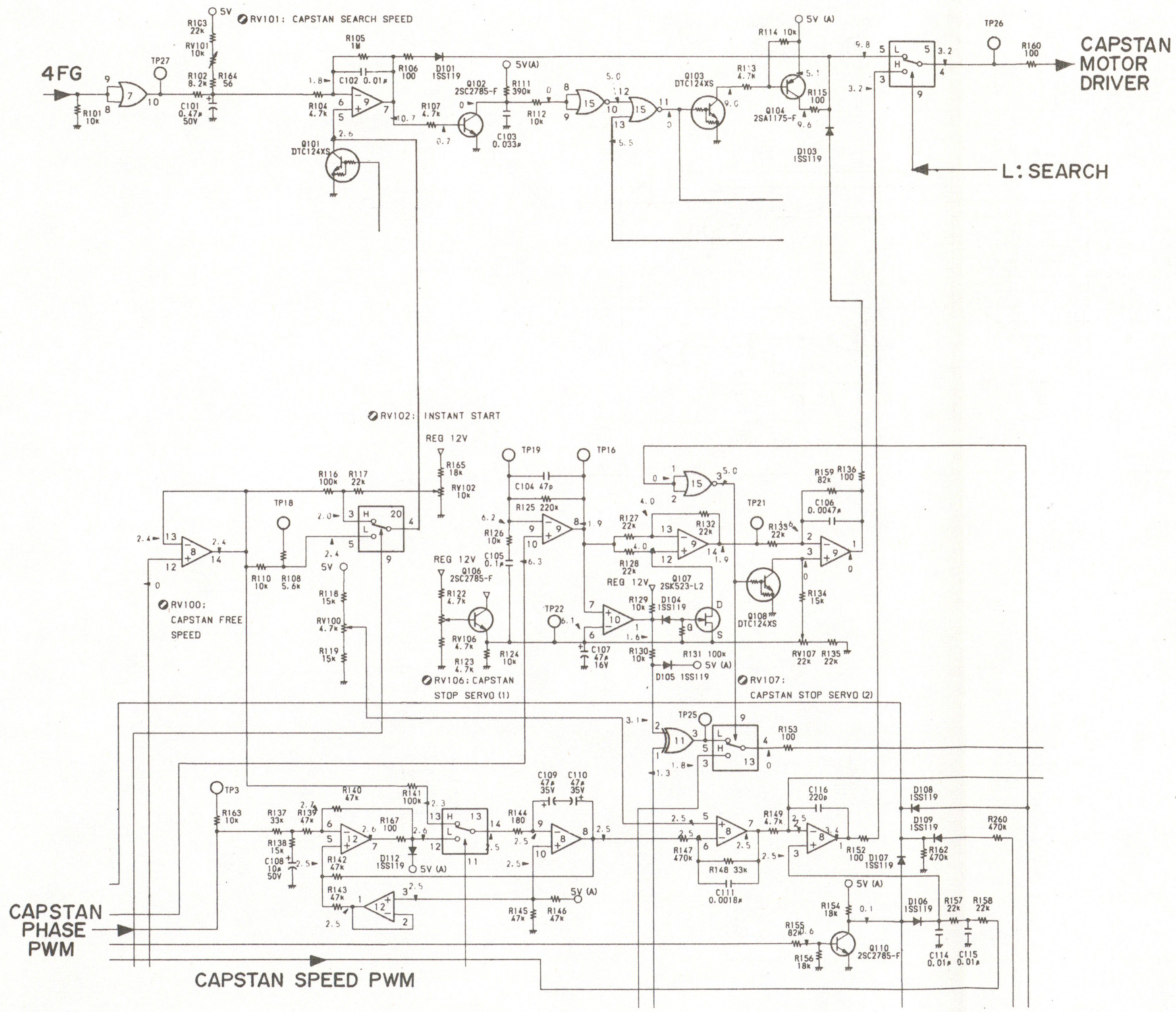


Fig. 3-5

In the SEARCH mode

The 4FG pulse at pin 19 of IC17 is passed through buffer IC7 and a low-pass filter consisting of R102 and C101 and then sent to comparator IC9. The signal voltages, corresponding to each speed from pins 25 through 30 of IC18, are fed to pin 12 of IC8. The buffer output is sent from pin 14. The resultant output is fed through switch IC20 to pin 5 of IC9 as a reference voltage. The signal at pin 5 of IC9 is compared with the input at pin 6, and the error voltage appears at pin 7 of IC9.

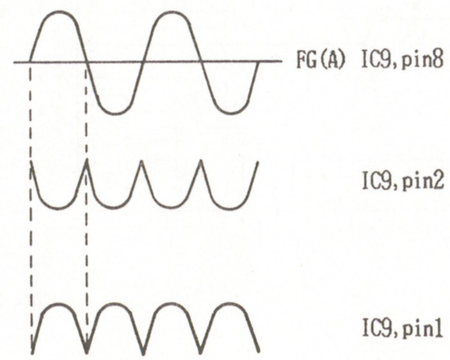
Capstan Stop Servo

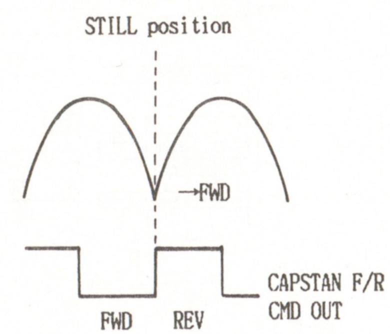
The servo is locked so that the tape should not be transported in the STILL mode.

As shown below, the FG (A) waveform is inverted by one half and added. The resultant waveform is then inverted as shown in the figure below.

When the capstan moves from the STILL position in the STILL mode, a force opposite to the capstan movement is applied to the motor to keep it at the former position.

A CAPSTAN F/R CMD OUT signal is generated using an EXCLUSIVE OR circuit after the FG (A) and FG (B) pulses are passed through the comparator.





Noiseless Still

When a STILL command is entered, the D/A OUT signal from IC18 becomes 0. When the capstan speed reaches 1/10 the normal speed, the speed is detected using pin 23 of IC17 (CX194). When a high-level signal is sent to pin 6 of IC18, the D/A OUT signal reaches 1/10 the normal speed.

When the capstan speed reaches 1/10 the normal speed in IC18, the 4FG pulse is counted from the trailing edge of a CTL signal. The count continues until still noise arrives below the picture, and then the D/A OUT signal becomes 0 to stop the capstan movement.

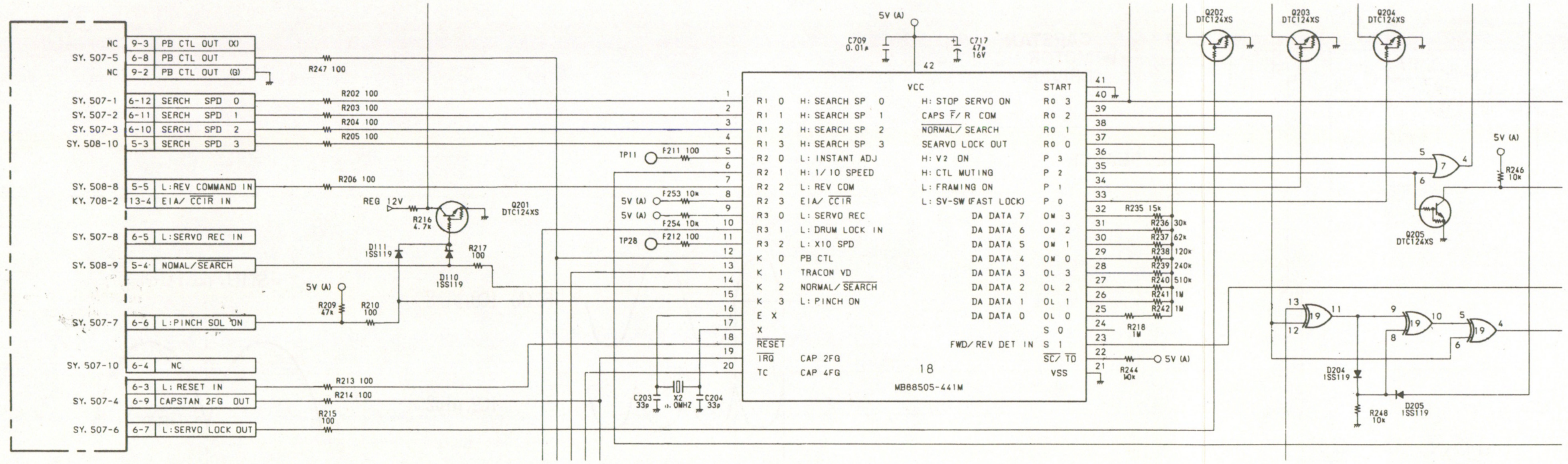


Fig. 3-6

SECTION 4
SYSTEM CONTROL CIRCUIT

OUTLINE (REFER TO Fig. 4-1)

The system controller consists of an SY board and a KY board.

Although the system control circuit in the Type V series contains discrete ICs, the system controller in VP-5020/5040 contains five one-chip microcomputers as shown in Fig. 4-1.

The block diagram of the system controller is shown below. The main functions of the one-chip microcomputers are as follows:

1. IC12/SY51 : Main microcomputer in the system control circuit — M1
2. IC7/SY-51 : Mechanical control for the motors and solenoids — M2
3. IC18/SV-74 : Instantaneous start control for the capstan — M3
4. IC/KY-91 : Key and LED controls — M4
5. IC14/SY-51 : Microcomputer for the remote control (RM-690) decoder — M5

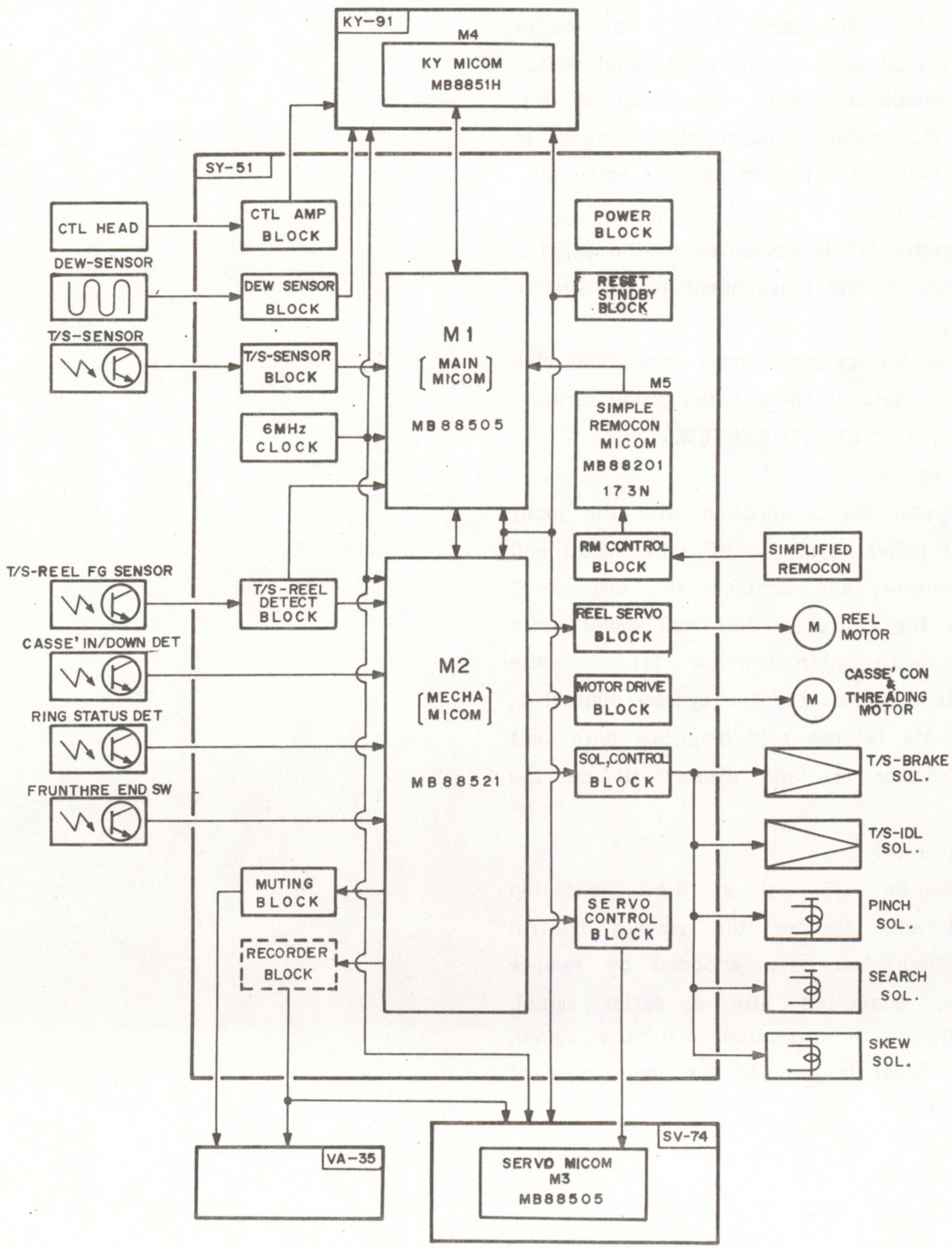


Fig. 4-1.

1. Microcomputer M1

Microcomputer M1 decodes information from microcomputer M2 (IC7/SY-51) and M4 (IC/KY-91) and produce commands to each microcomputer.

Microcomuter M1 is supplied with a lot kinds of information. They are, the front panel function key signals sent from microcomputer M4, switch input signals, information of remote controller RM-690 sent from microcomputer M5, and the tape beginning and tape end sensor outputs.

2. Microcomputer M2

Microcomputer M2 is a slave for microcomputer M1. The servo data is supplied to microcomputer M2. The servo data is the motor statuses, sensor LED outputs, and mechanical switch signals. Communicating with microcomputer M1, microcomputer M2 produces and supplies comands to the mechanical parts, the motors and the solenoids.

3. Microcomputer 3

Microcomputer M3 is dedicated to the capstan servo control system and independent of the system control circuit.

It controls the capstan phase servo and also locks the initial phase of the capstan phase servo. (For details, refer to SERVO SYSTEM.)

4. Microcomputer M4

Microcomputer M4 is supplied with the input from the front panel keys, the PB CTL signal and DEW sensor output, and controls the display of information by the LEDs on the front panel while communicating with microcomputer M1. While performing self diagnosis for the system control 2, microcomputer M4 latches self diagnosis data sent from microcomputer M1 and displays it on the LEDs.

5. Microcomputer M5

Microcomputer M5 is a 4-bit one-chip microcomputer and decodes the remote control instruction, which has been encoded by remote controller and converted into a serial signal. Decoded by the M5, it is obtained a parallel signal. The resultant signal is sent to the input port of microcomputer M1.

4-1. POWER SUPPLY (REFER TO Fig. 4-2.)

The power supply circuit on the SY-51 board (Q35 and D20 through D24) generates the REG 5V dc (SP) and backup 5V dc using the REG 7V dc and REG 12V dc which are supplied from the switching regulators.

The reference voltage is obtained by dividing the regulated 12V dc through resistors R159 and R160. Using this reference voltage, the stabilized 5V dc is obtained. If it is short-circuited between the REG 5V dc and the ground, the linc IC resistor R192, whose constant rate is at 1.0A, opens up to protect Q35 from heating.

The backup 5V dc and regulated 5V (SP) power supplies are described below.

4-1-1. Backup 5V DC Power Supply

The backup 5V dc power supply is used for the KY microcomputer. When the backup 5V dc power supply is used, CTL data stored in the KY microcomputer is held for 3 days with the power off state.

4-1-2. Regulated 5V DC (SP) Power Supply (Refer to Fig. 4-3.)

The regulated 5V dc (SP) power supply is used for the power-on reset circuit and detects the reference voltage when the KY microcomputer enters the backup mode. When the power is turned off, the REG 5V dc (SP) power supply takes longer time to fall down than that of the REG 5V dc power supply.

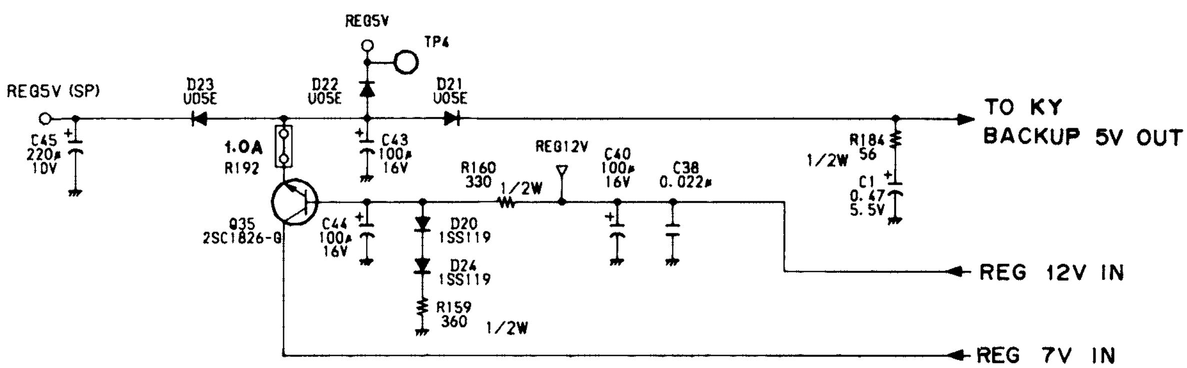


Fig. 4-2

4-2. RESET CIRCUIT

4-2-1. Power-on Reset Circuit

The power-on reset circuit (IC11 and Q23) resets the five microcomputers in the VTR during the power-on reset sequence.

4-2-2. Power Switch ON/OFF Circuit (IC15)

The REG 5V dc power supply output may become lower than 4.5V dc when the power switch is successively turned on, off, and on. The microcomputer operation cannot be assured with such a low-voltaged dc. To prevent this, the power switch on/off circuit resets the microcomputer when the drop voltage is detected. (Refer to Fig. 4-4.)

When the power switch is turned off, the REG 5V dc and 7V dc power supply outputs drop while the REG 5V dc (SP) power supply stays at 5V dc for a while. When the reference voltage (2.75V) appears at pin 2 of IC15, the REG 5V dc and 7V dc power supply outputs drop until the REG 5V dc power supply output becomes 4.5V dc. When the REG 5V dc power supply output is 4.5V dc, the REG 7V dc power supply output becomes approximately 5.5V dc. The power switch on/off circuit detects this 5.5V dc and resets the microcomputers.

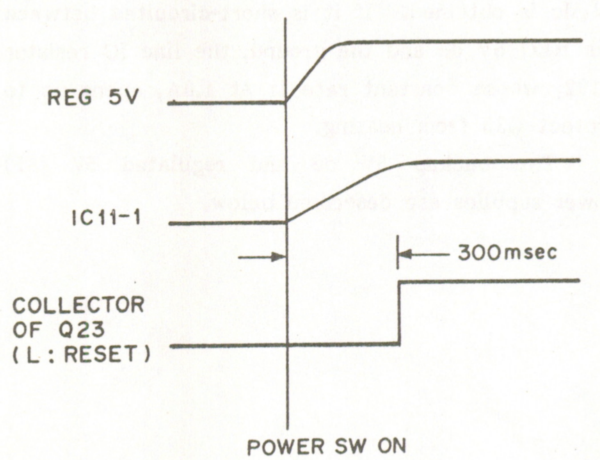


Fig. 4-3

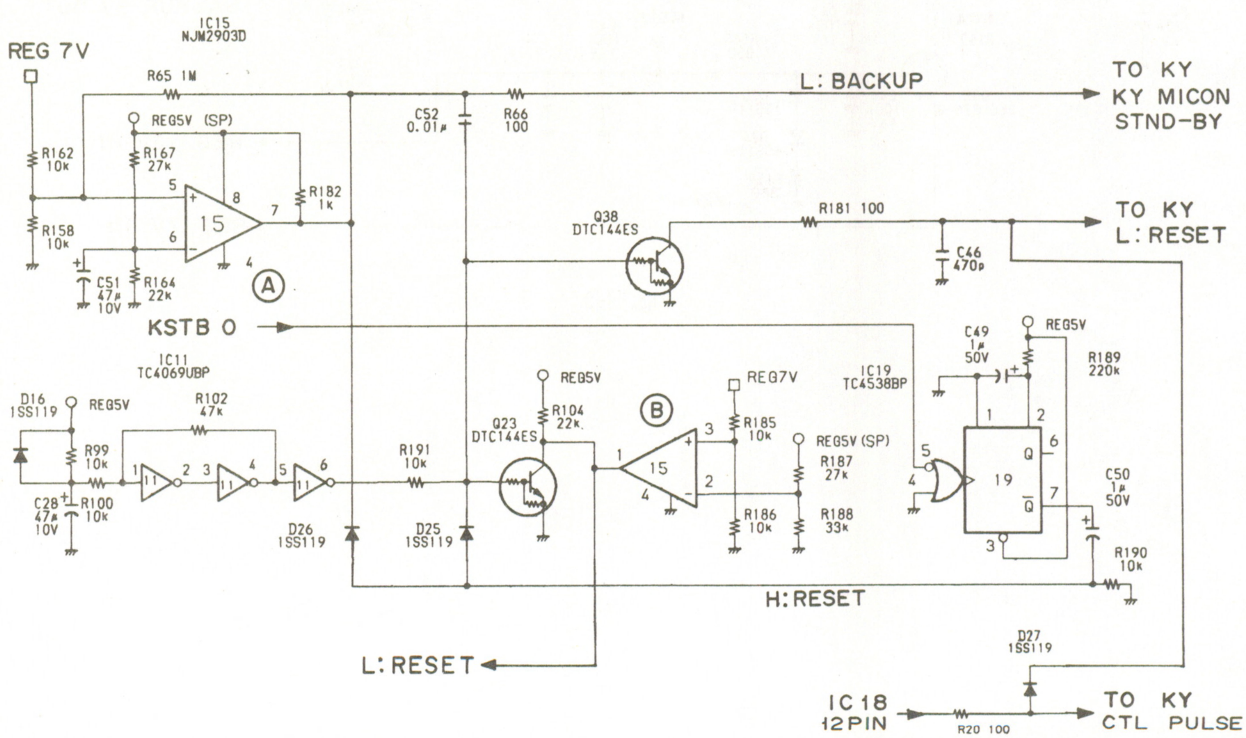


Fig. 4-4

4-3. STANDBY DETECTION CIRCUIT (REFER TO FIG. 4-4.)

The KY microcomputer (IC1/KY) which is operated on backup 5V dc, so the data on the CTL counter is kept even when the power switch is turned off. The microcomputer enters the STANDBY mode to reduce the power dissipation. The KY microcomputer consumes approximately 0.1μA in the STANDBY mode. Data can be stored until the supply voltage becomes 3.5V dc.

If the REG 5V dc and 7V dc supply voltages decrease when the power switch is turned off, microcomputers M1 and M2 are reset by the power switch on/off reset circuit (Refer to Fig. 4-5).

If the REG 5V dc and 7V dc supply voltages decrease when the power switch is turned off, microcomputers M1 and M2 are reset by the power switch on/off reset circuit (Refer to Fig. 4-5).

If the voltage at pin 5 of IC15 becomes 2.24V or lower, the signal at pin 1 of IC15 goes low and the KY microcomputer enters the STANDBY mode.

If the microcomputer is released from the STANDBY mode, the KY microcomputer is reset by C52.

If the STANDBY mode is detected by IC15, the reset signal is inhibited by D26 and the microcomputer cannot be reset even if IC19 outputs an erroneous signal.

4-4. STOP DETECTION CIRCUIT (REFER TO FIG. 4-4.)

When microcomputer M1 stops communicating with the KY microcompter, communication strobe signal K STB 0 is also stopped. Detecting this state, IC19 resets the microcomputers. If the K STB 0 signal at pin 5 of IC19 is lower than 220ms, the signal at pin 7 of IC19 goes high.

4-5. FR CTL AMPLIFIER CIRCUIT (REFER TO FIG. 4-6.)

The PB CTL signal fed from the FR CTL head is amplified by the amplifier IC2. The amplified signal is sent through the schmit circuit IC1 to the KY boar, as the CTL count pulse. It is then counted by the KY microcomputer.

The bias voltage is supplied from pin 1 of IC1 to pin 6 of IC1.

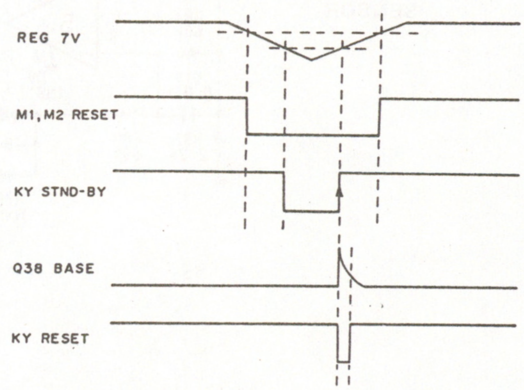


Fig. 4-5

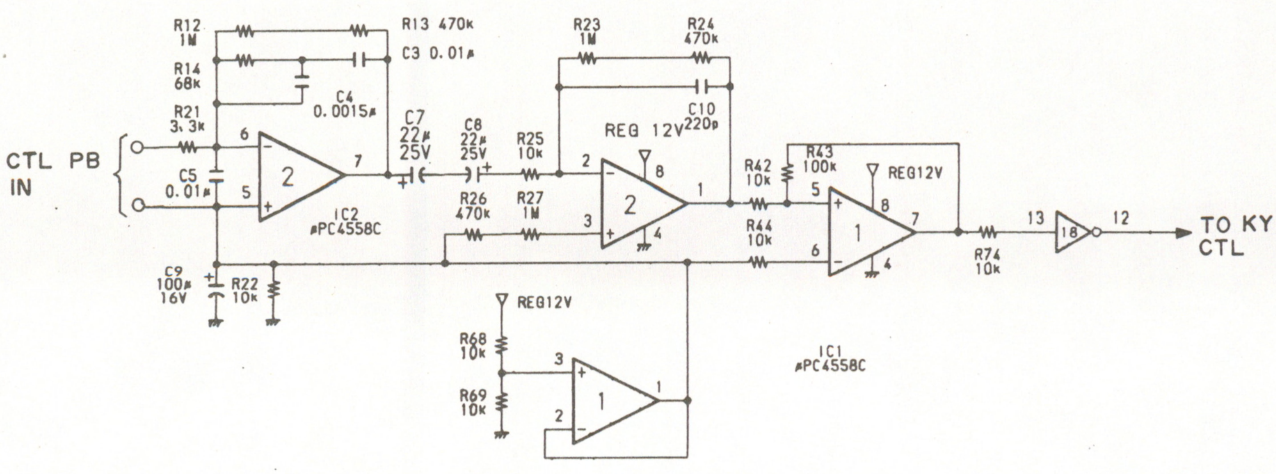


Fig. 4-6

4-6. CONDENSATION DETECTION BLOCK (REFER TO FIG. 4-7.)

IC5 comprises the oscillation circuit. Unless dew condensation is detected, a strong negative feedback is established by R87 and oscillation cannot occur. If dew condensation is detected, one of leads of capacitor C20 is connected to ground and the negative feedback is suppressed, the oscillation occurs. The oscillation circuit output is detected by D10 and D11, and then smoothed by capacitor C24. The smoothed signal is fed to transistor Q20, and turns it on.

When dew condensation is detected, Q20 turns on. The L AUTO OFF signal, which is sent from the SY board to the KY board, lights the AUTO OFF lamp. This signal is also fed to the KY microcomputer. The VTR enters the EJECT mode while microcomputer M1 is operated, and the cassette is ejected. The drum then starts rotating.

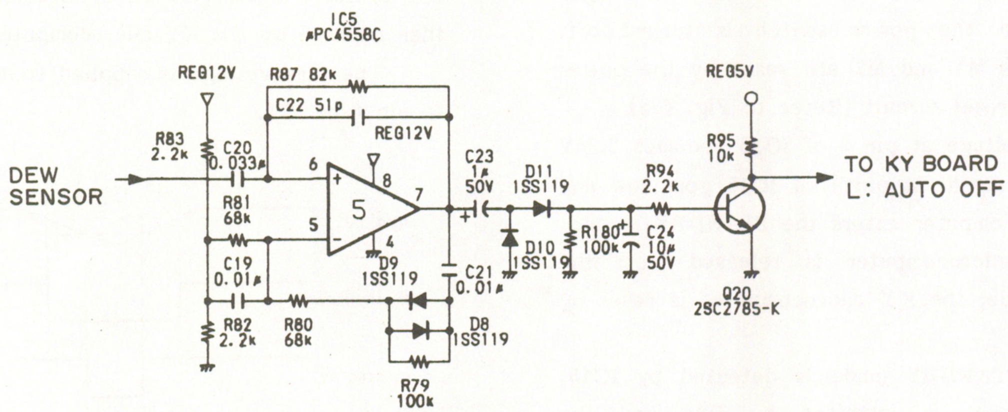


Fig. 4-7

4-7. TAPE BEGINNING/TAPE END DETECTION CIRCUITS (REFER TO FIG. 4-8.)

The tape end and tape beginning detection circuit consists of IC8 and Q31. The reference voltage at pin 3 of IC8 is approximately 8.9V DC, and that at pin 6 is approximately 3.1V DC.

4-7-1. When the Tape End Is Detected

The signal voltage at TP2 becomes approximately 11V DC. The signal at pin 1 of IC8 goes low and that at pin 7 of IC8 goes high. When the tape end mark is detected, the VTR enters the REWIND mode.

4-7-2. When the Tape Beginning Is Detected

The signal voltage at TP2 becomes approximately 1.0V DC. The signal at pin 1 of IC8 goes high and that at pin 7 of IC8 goes low. When the tape beginning mark is detected, the VTR enters the SHORT FF mode. The tape runs forwards for 128 reel FGs, then the VTR enters the STOP mode. The amount of 128 reel FGs is the same as that of a conventional VTR.

4-7-3. When neither the Tape Beginning nor Tape End Are Detected

(Normal state)

The signal voltage at TP2 becomes approximately 6V DC. The signal at pin 1 of IC8 goes high, and that at pin 7 of IC8 goes high.

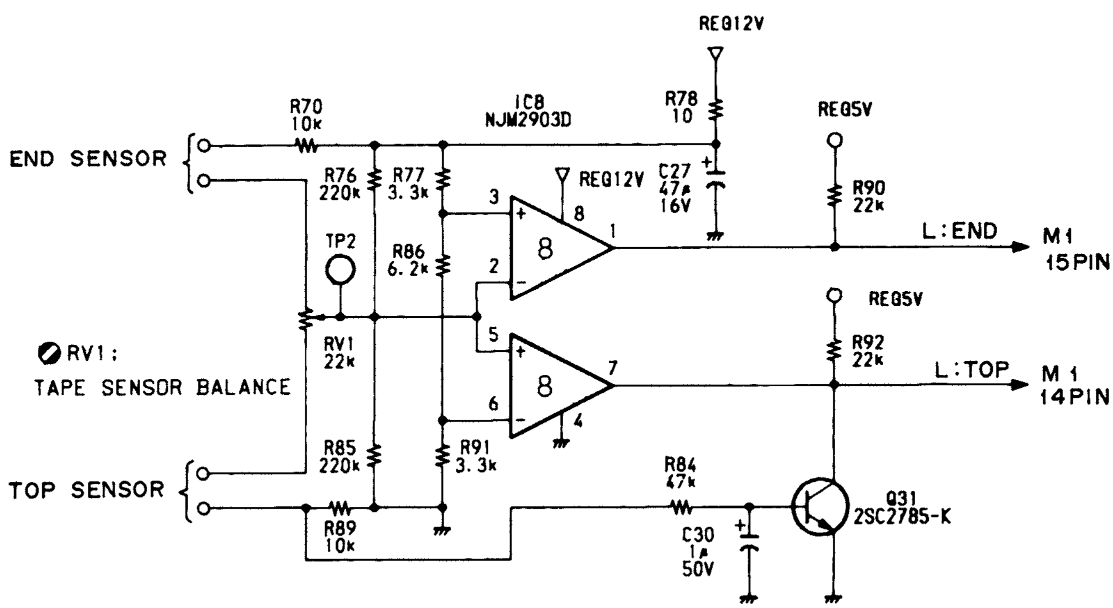


Fig. 4-8

4-7-4. When both the Tape Beginning and Tape End Are Detected

The signal voltage at TP2 becomes approximately 6V DC. The signals at pin 1 and pin 7 of IC8 go high, just same as the normal state. However, transistor Q31 turns on to forcibly detect the tape beginning.

(1) If the leader tape is detected at the beginning of the tape by both the tape beginning and tape end detection circuits, Q31 turns on and detects the tape beginning. The VTR enters the SHORT FF mode.

(2) If the leader tape is detected at the end of the tape by both the tape beginning and tape end detection circuits, the VTR enters the FF mode. The stopped reel is detected at the end of the tape, and the VTR enters the STOP mode. At this time, only the EJECT key is available.

4-8. REEL ROTATION DETECTOR (REFER TO FIG. 4-9.)

The reel FG signal waveforms of the take-up and supply reels are shaped by Q4 and Q8, and then fed to monostable multivibrators. If the reel stops rotating or rotates at an extremely low speed, the signals at pins 6 and 10 of IC3 go low. These signals are fed to microcomputer M2 and are used to detect the rotation of the reel table or the slack. The reel FG signal for the take-up reel is directly sent from Q8 to microcomputer M1. This signal is controlled in the SHORT FF mode, and then the VTR enters the STOP mode.

4-9. REMOTE CONTROL CIRCUIT

The remote control circuit consists of IC14, Q24, Q27, Q28, and Q29. The remote controller communicates with the VTR through two signal lines, the power supply + serial data line and the common line. The remote control command sent in serial format is encoded by the remote controller. The remote control command is a 5V DC signal modulated at 40 KHz. Serial signal sent from the remote controller is amplified by Q28, then shaped by Q27 and Q29. The shaped signal is then fed to pin 9 of IC14, where it is decoded into a six-bit parallel signal. The six-bit parallel signal is fed to microcomputer M1 (IC12). The function key signal generated on the front panel is fed to the KY microcomputer and sent to microcomputer M1 on the SY board.

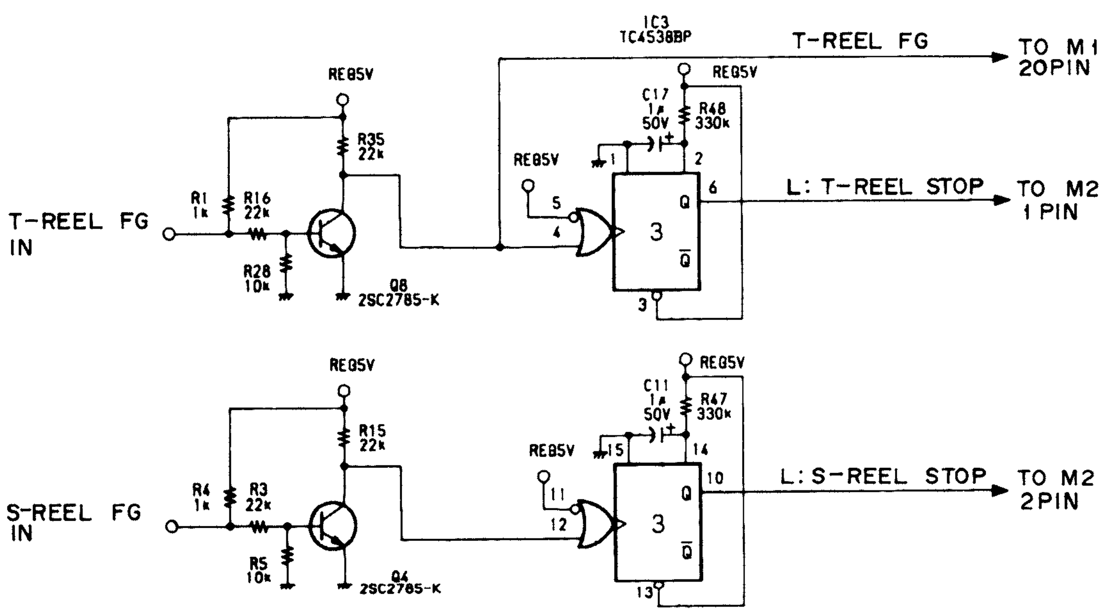
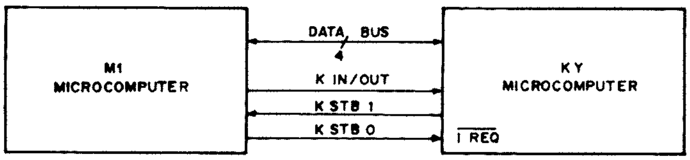


Fig. 4-9.

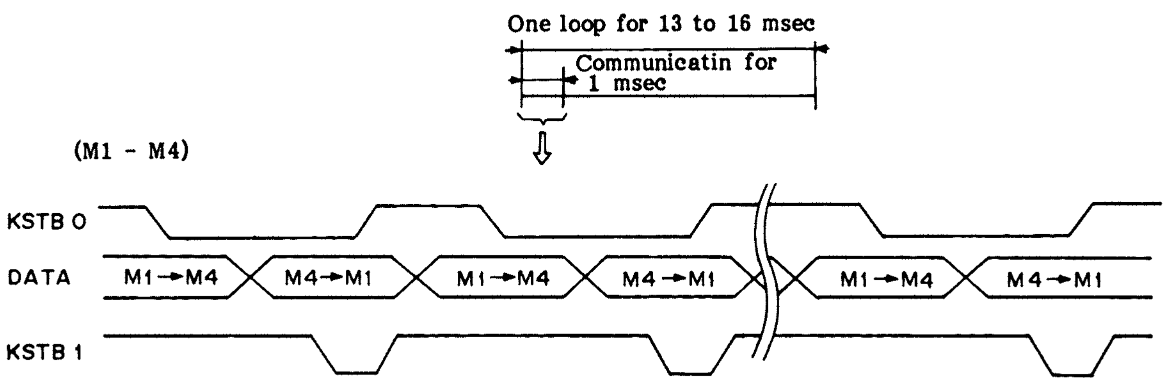
4-10. INTERFACE BETWEEN MICROCOMPUTER M1 AND MICROCOMPUTER KY

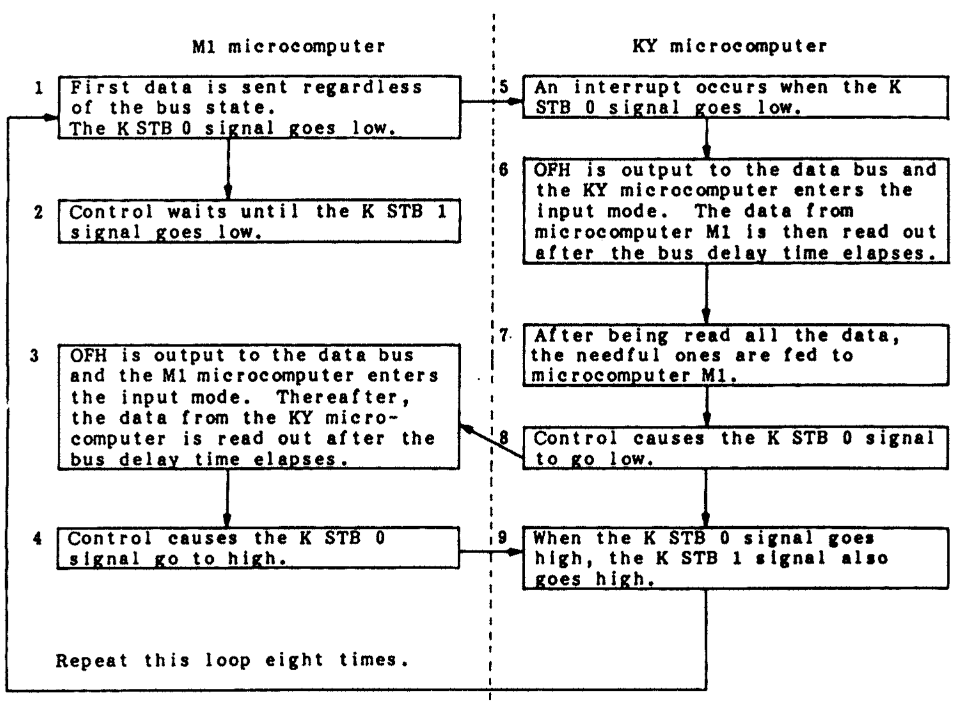
Microcomputer M1 communicates with the KY microcomputer via four signal lines every 13 to 16 msec, and a loop for approximately 1 ms is established every 13 to 16 msec.



- K STB 0 : When an interrrupt signal for the K STB 0 is sent from microcomputer M1 to the KY microcomputer, communication starts.
- K STB 1 : When the data is sent from the KY microcomputer to microcomputer M1, the K STB 1 strobe signal is sent.
- K IN/OUT : It confirms that the data supplied to the KY microcomputer corresponds with the microcomputer M1 output. This prevents data-shifting while being transferred between these microcomputers.
- DATA BUS :Bidirectional four-bit data line

The communication sequence between microcomputer M1 and the KY microcomputer is shown below.





4-11. REEL MOTOR DRIVE CIRCUIT (REFER TO FIG. 4-10.)

The reel motor drive circuit is a current drive type which is the same as that of the conventional Type V. This circuit consists of a tension servo circuit and a torque servo circuit. The following signals are output from microcomputer port IC7, and the reel servo circuit is controlled by these signals.

H: REEL STOP	at pin 58
H: REEL STILL	at pin 59
H: REEL FWD	at pin 60
H: REEL REV	at pin 61
H: REEL FF REW	at pin 24

When the signal at pin 58 is high, Reel Stop signal is sent. The VTR enters the STOP mode.

A DC voltage is fed through D4 to Q14 to turn on Q14, and no voltage is applied to IC4. Thus, no drive torque is applied to the reel motor.

When the signal at pin 59 is high, Reel Still signal is sent. The VTR operates in the PLAY PAUSE or SEARCH PAUSE mode.

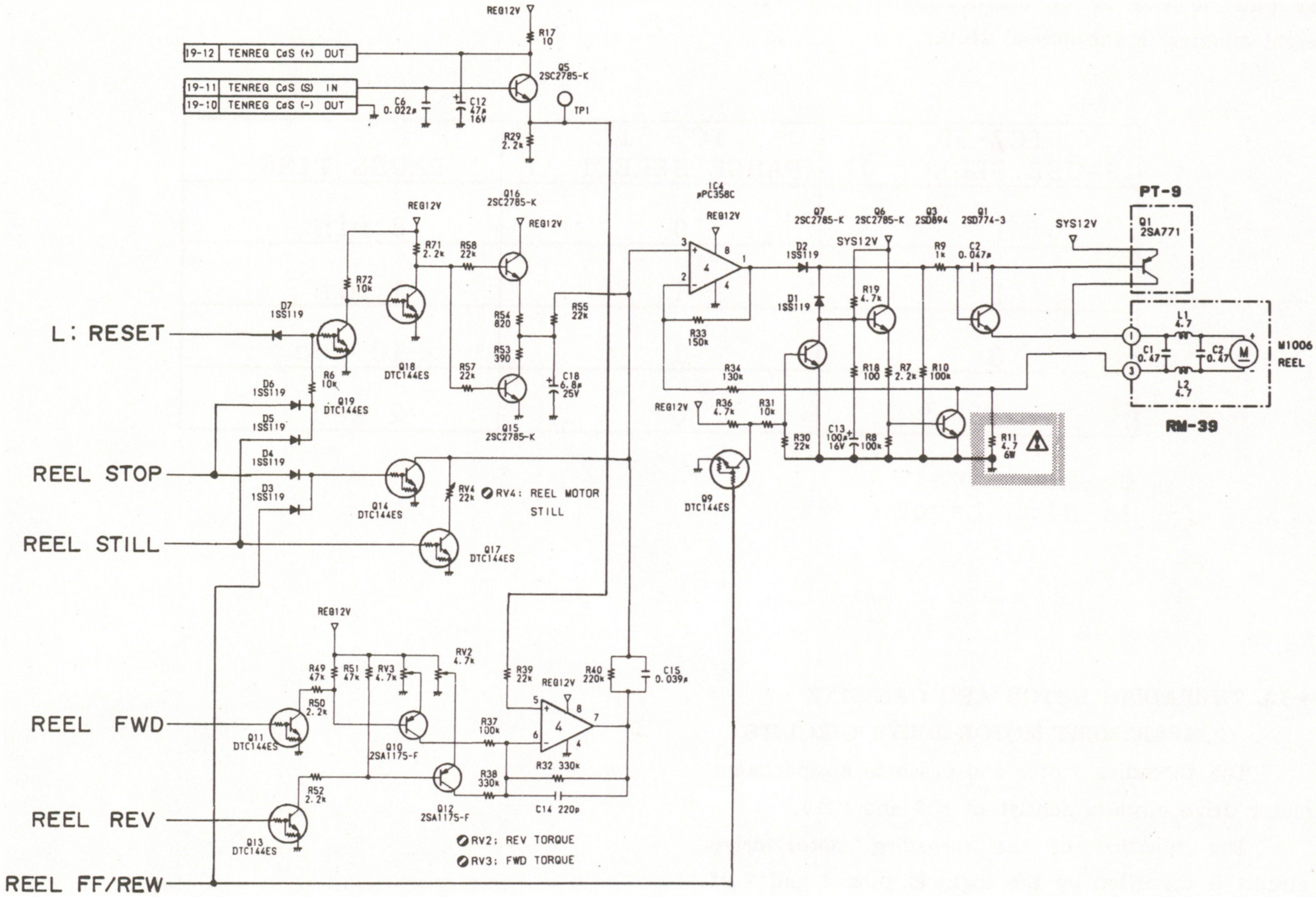
A DC voltage is fed through D5 to Q19 to turn on Q19 and Q17. A voltage generated by Q16 and Q15 and another voltage appearing across RV4 are applied to IC4 so that the reel motor is driven to tension the tape.

When the signal at pin 60 is high, Reel FWD signal is sent. The VTR operates in the PLAY or SEARCH FWD mode.

A DC voltage is fed to Q10 and Q11 to turn on these transistors. The DC voltage established by RV3 is fed to pin 6 of IC4. A DC voltage fed from the tension detector in the tension regulator is fed to pin 5 of IC4, the voltages appearing at pins 5 and 6 of IC4 are compared to obtain an error voltage, and the error voltage is fed to the reel motor. The current flowing through the reel motor is detected by R11, and the voltage across R11 is fed back to pin 2 of IC4 so that a constant torque can be obtained.

When the signal at pin 61 is high, Reel REV signal is sent. The VTR operates in the SEARCH REV mode.

A DC voltage is fed to Q12 and Q13 to turn on these transistors. The reference voltage is determined by RV2 in the same manner as in the REEL FWD mode. The reel servo circuit consists of the tension detection circuit.



19-12 TENREG CdS (+) OUT
19-11 TENREG CdS (S) IN
19-10 TENREG CdS (-) OUT
L: RESET
REEL STOP
REEL STILL
REEL FWD
REEL REV
REEL FF/REW
PT-9
RM-39
M1006
REEL
RV4: REEL MOTOR STILL
RV2: REV TORQUE
RV3: FWD TORQUE

Fig. 4-10

4-12. PAUSE TIME SELECTION

The PAUSE time is determined by the logic at pins 50 and 51 of microcomputer IC7. It is eight minutes in the normal state.

IC7-50 (PAUSE SELECT 0)	IC7-51 (PAUSE SELECT 1)	PAUSE TIME
1	0	8 min
1	1	1 min
0	1	10 sec
0	0	2 sec

0: Low Level
1: High Level

4-13. THREADING MOTOR AND CASSETTE COMPARTMENT MOTOR DRIVE CIRCUITS

The threading motor and cassette compartment motor drive circuits consist of IC9 and IC10.

The function of the threading motor drive circuit is specified by the logic at pins 4 and 6 of those ICs.
(Table.)

INPUT		OUTPUT				
PIN 4	PIN 6	PIN 7	PIN 3		IC 9	IC 10
0	0	X	X	NO OPERATION	———	———
1	0	1	0	ROTATION	CC DOWN	THREADING
0	1	0	1	REUESE ROTATION	CC UP	UNTHREADING
1	1	0	0	BRAKE	BRAKE	

0: Low Level
1: High Level
X: Don't Care

4-14. SELF DIAGNOSIS

4-14-1. Outline

The VP-5020/5040 has a self diagnosis function. Whether the trouble is caused by the microcomputer or not can be determined by the self diagnosis function. This enables the VTR with a microcomputers to find the cause of the trouble easily.

How to use the microcomputer in the VP-5020/5040 and how to operate the self diagnosis function are described below.

Five microcomputer functions:

One-chip microcomputers M1 and M2, which include the respective memories and I/O ports, are used for the master controls. Microcompter M3 is for controlling the capstan motor, the M4 is for controlling the display, and the M5 is for decoding the remote control signal.

. Self-diagnosis method

Information at the I/O port in each step is compared with the table contents, which have been prepared. The difference, if any, can be then found. Whether the trouble is caused by the microcomputer or not can be found, in this way.

The VTR has a mechanism control and a communication control. The self diagnosis can effectively be used to analyze any failures of the mechanism control. The ROM consists of a system control area and an area which can be used for the self diagnosis. The self-diagnosis area stores the program to latch information at the respective ports and to display them on the front panel. Information from microcomputer M1, which obtains the results of the self diagnosis, can be displayed by the LEDs on the front panel using microcomputer M4.

4-14-2. Display of Self Diagnosis Function

Set switch SW1 on the SY-51 board to ON to display the result of the self diagnosis.

I/O data at the I/O port of the microcomputer is displayed every four bits in each test address as described on page 4-16 when the result of the self diagnosis is displayed. Press the RESET button to display the test address. Press the MARK switch while pressing the RESET button to change the LSB of the test address as follows:

→ 0 → 1 → 2 → .... → 9 → L → H → P → R → –(Minus) → (Blank) →

When the MARK B switch is pressed while pressing the RESET button, the MSB of the test address changes as follows:

→ 0 → 1 → 2 →

The test address is up to 26 in hexadecimal notation. Data (digits 1 through 4) of the test address (pages 4-16 through 4-18) is displayed by the LEDs using the RESET, MARK A, and MARK B switches. A logic of each signal is high, this means "1", and the low, "0". The logic value is changed in accordance with the operating states of the VTR. Therefore, the H: DRUM STOP signal at test address "01" can be observed by the following processes.

[Operation]	[LED display]	
	(CTL display)	
	↓	
SW1/SY-51 — ON	1 1 0 0	(DIAGNOS-TICS MODE)
↓	↓	
Press the RESET button.	0 0	(TEST ADDRES=00)
↓	↓	
Press the MARK A button once while pressing the RESET button.	0 1	(TEST ADDRESS=01)
↓	↓	
Release the RESET button.	1 1 1 1	(Data for 01)
	⇑	
	H: DRUM STOP SIGNAL	

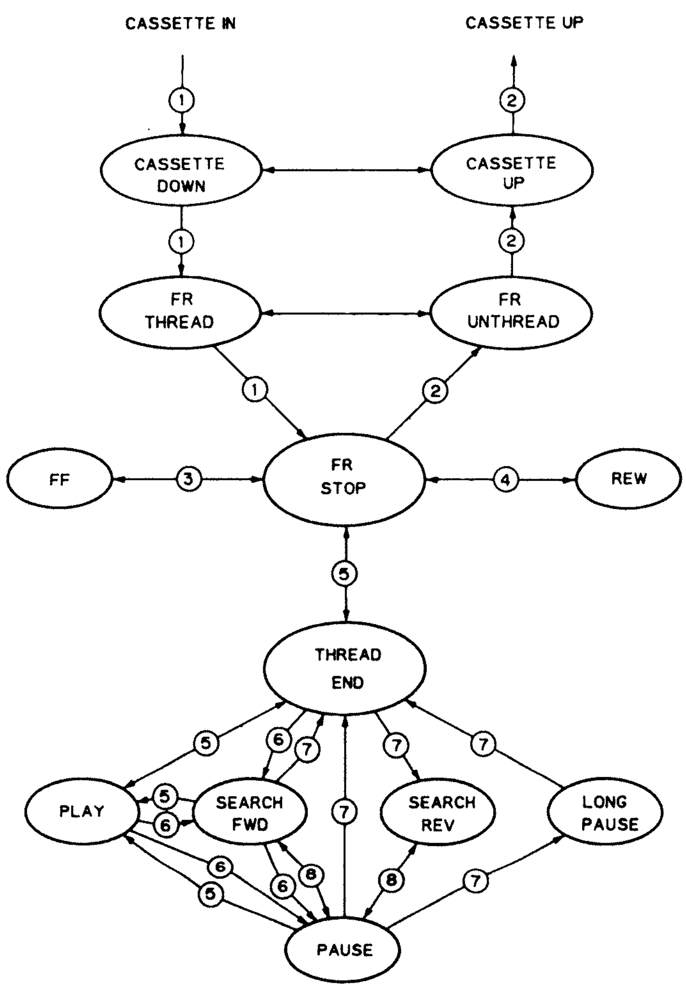
If the drum is stopped at this time, the MSB is high. That is, the value is logic 1. When the cassette is inserted and the VTR is put into the PLAY mode, this value becomes logic 0. Logic 0 indicates the order to rotate.

The output signals on pages 4-19 through 4-34 are thus output.

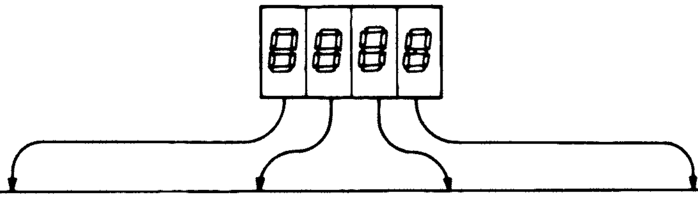
4-14-3. Troubleshooting

Troubleshooting with self diagnostic function is described below. The mode change in the VP-5020/5040 mechanism is shown in the chart. The location where any trouble occurred, and any faulty mechanism (the motor or solenoid) operation can be confirmed by referring to the chart. After it is found where the trouble occurs, see the timing chart. It describes the mode change. The input and output signals for the microcomputer in each mode are indicated in the timing chart. When there are any motors or solenoids which are not operating normally, the output signal lines are observed by the LEDs. Whether the output signals change in accordance with the timing chart or not is checked. If the output signal of the microcomputer is satisfactory, the output signal of the next microcomputer is checked. This process is continued. If any output signal does not change in accordance with the timing chart, check the cause of the failure by referring to the circuit diagram. The timing chart describes the input/output signal names, the test addresses for each signal to be displayed, the number of digits, and the pin names of the microcomputer from or to which signals are sent or supplied. For instance, H: DRUM STOP signal is specified as "01-DIGIT 1". If the test address is "01", the MSB (digit 1) of this test address is displayed as "01-DIGIT 1". Thus, whether or not the signals change in accordance with the timing chart is checked during operation.

The mode changing of the VP-5020/5040 mechanism



Note: Numbers in the illustration indicate the timing chart numbers.



TEST ADDRESS	DATA DISPLAYED DIGIT 1	DIGIT 2	DIGIT 3	DIGIT 4	INPUT/OUTPUT PORT NAME ON THE MICRO PROCESSOR	
00	CAPSTAN CMD FWD/$\overline{\text{REV}}$ (1=FWD CMD (0=REV CMD	NORMAL/$\overline{\text{SEARCH}}$ (1=NORMAL (0=SEARCH MODE	0	0	E1	OUT/IC7 on SY-51
01	H : DRUM STOP CMD (1=DRUM STOP (0=DRUM ROTATE	1	1	1	E2	OUT/IC7 on SY-51
02	CTL COUNT UP/$\overline{\text{DOWN}}$ (1=COUNT UP (0=COUNT DOWN	L : SKEW SOL. ON (1= OFF (0= ON	1	1	E3	OUT/IC7 on SY-51
03	H : REEL REV 1=SEARCH REV MODE	H : REEL FWD 1=PLAY or SEARCH FWD MODE	H : REEL STILL 1=PLAY PAUSE or SEARCH PAUSE	H : REEL STOP 1=STOP MODE	P	OUT/IC7 on SY-51
04	H : REEL FF/REW (1=FF or REW MODE (0=other mode	L : SEARCH SOL.ON (1=OFF (0=ON	L : PINCH SOL.ON (1=OFF (0=ON	1	O	OUT/IC7 on SY-51
05	L : T-BRAKE SOL.ON (1=OFF (0=ON	L : S-BRAKE SOL.ON (1=OFF (0=ON	L : T-IDLER SOL.ON (1=OFF (0=ON	L : S-IDLER SOL.ON (1=OFF (0=ON	E0	OUT/IC7 on SY-51
06	SEARCH SPEED DATA (NOTE 1)				R2	OUT/IC7 on SY-51
07	L : CASSETTE COMPARTMENT UP CMD 0=UP	L : CASSETTE COMPARTMENT DOWN CMD 0=DOWN	L : THREAD MOTOR ON 0=THREAD	L : UNTHREAD MOTOR ON 0=UNTHREAD	R3	OUT/IC7 on SY-51
08	0	L : FR-UNTHREAD POSITION	H : CASSETTE DOWN 1=DOWN (NOTE 2)	H : CASSETTE IN 1=INSERTED	K	IN/IC7 on SY-51
09	H : DRUM STOP (1=STOP (0=ROTATE	H : REEL STOP (1=STOP (0=ROTATE	H : T-IDLER ON (1=ON (0=OFF	H : T-REEL STOP (1=STOP (0=ROTATE		
OL	L : CAPSTAN STOP (1=ROTATE (0=STOP	CAPSTAN FWD/$\overline{\text{REV}}$ (1=FWD (0=REV	UNTHREAD END (NOTE 3)	THREAD END	R1	IN/IC7 on SY-51
OH	0	0	PAUSE SELECT-1 0 (NOTE 4)	PAUSE SELECT-0 1	E4	IN/IC7 on SY-51
OP	L : DRUM ROTATE (1=STOP (0=ROTATE	L : CASSETTE CONNECT 0	L : SLACK DET : OFF (NOTE 5)	0	E5	IN/IC7 on SY-51
OR	RING SLACK ERROR MASSAGE (NOTE 6) The condition of VP-5020 is detected by IC7/SY-51 board when the ring slack occurs. RING SLACK means does not rotate the threading ring.					
O-	0	0	0	0		
O (Blank)	0	0	0	0		

10	0	0	0	0
11	0	0	0	0
12	0	0	0	0
13	0	0	0	0
14	0	0	0	0
15	0	0	0	0
16	0	0	0	0
17	0	0	0	0
18	REMOTE CONTROL CODE FROM RM-690 (NOTE 8)			
19	1	1	1	1
1L	1	1	1	1
1H	1	1	1	1
1P	1	1	1	1
1R	1	1	1	1
1-	1	1	1	1
1 (Blank)	1	1	1	1
20	REEL SLACK ERROR MASSAGE (NOTE 7) The condition of VP-5020 is detected by IC12/SY-51 board When the reel slack occurs. REEL SLACK means does not rotate the reel motor.			
21	0	0	0	0
22	0	0	0	0

23	0	0	L : VIDEO MUTE (1=VIDEO is OUTPUT (0=VIDEO is MUTED	H : AUDIO MUTE (1=AUDIO is MUTE (0=AUDIO is OUTPUT
24	1	0	0	0
25	0	0	0	0
26	0	0	0	0

NOTE 1 SEARCH SPEED DATA

DATA DISPLAYED	TAPE SPEED
0 0 0 0	NOISE LESS STILL
0 1 0 1	x 1
0 1 1 1	x 5
1 0 0 1	STILL

NOTE 2 SLACK DET:OFF/DIAGNOSTICS MODE

SLACK DET:OFF	DIAGNOSTICS	VTR CONDITION
1	1	NORMAL
0	1	SLACK DETECTION IS DISABLED
1	0	DIAGNOSTICS MODE (NORMAL TAPE SPEED)
0	0	DIAGNOSTICS MODE, SLACK DETECTION IS DISATIED X 1/2 NORMAL TAPE SPEED

NOTE 3 THREAD END/UNTHREAD END

UNTHREAD END	THREAD END	THREADING RING POSITION
1	1	Between CASSETTE-IN and FR-STOP
0	1	THREAD END position
0	0	Between FR-STOP and THREAD END
1	0	FR-STOP position

NOTE 4 PAUSE SELECT-1/PAUSE SELECT-0

PAUSE SELECT-1	PAUSE SELECT-0	PAUSE TIMER
0	1	8 min
1	1	1 min
1	0	10 sec
0	0	2 sec

NOTE 5 SLACK DETECT

- While shorting between TP 3 and GND(E1) on The SY-51 board, SLACK Detector does not operate. Normal state is "H".

NOTE 6 RING SLACK ERROR MASSAGE

DATA DISPLAYED	CONDITION
0 0 0 0	RING SLACK does not occur
0 0 0 1	CASSETTE DOWN → FR-STOP
0 0 1 0	FR-STOP → THREAD END
0 0 1 1	THREAD END → FR-STOP
0 1 0 0	FR-STOP → CASSETTE DOWN
0 1 0 1	FR-STOP → CASSETTE DOWN

NOTE 7 REEL SLACK ERROR MASSAGE

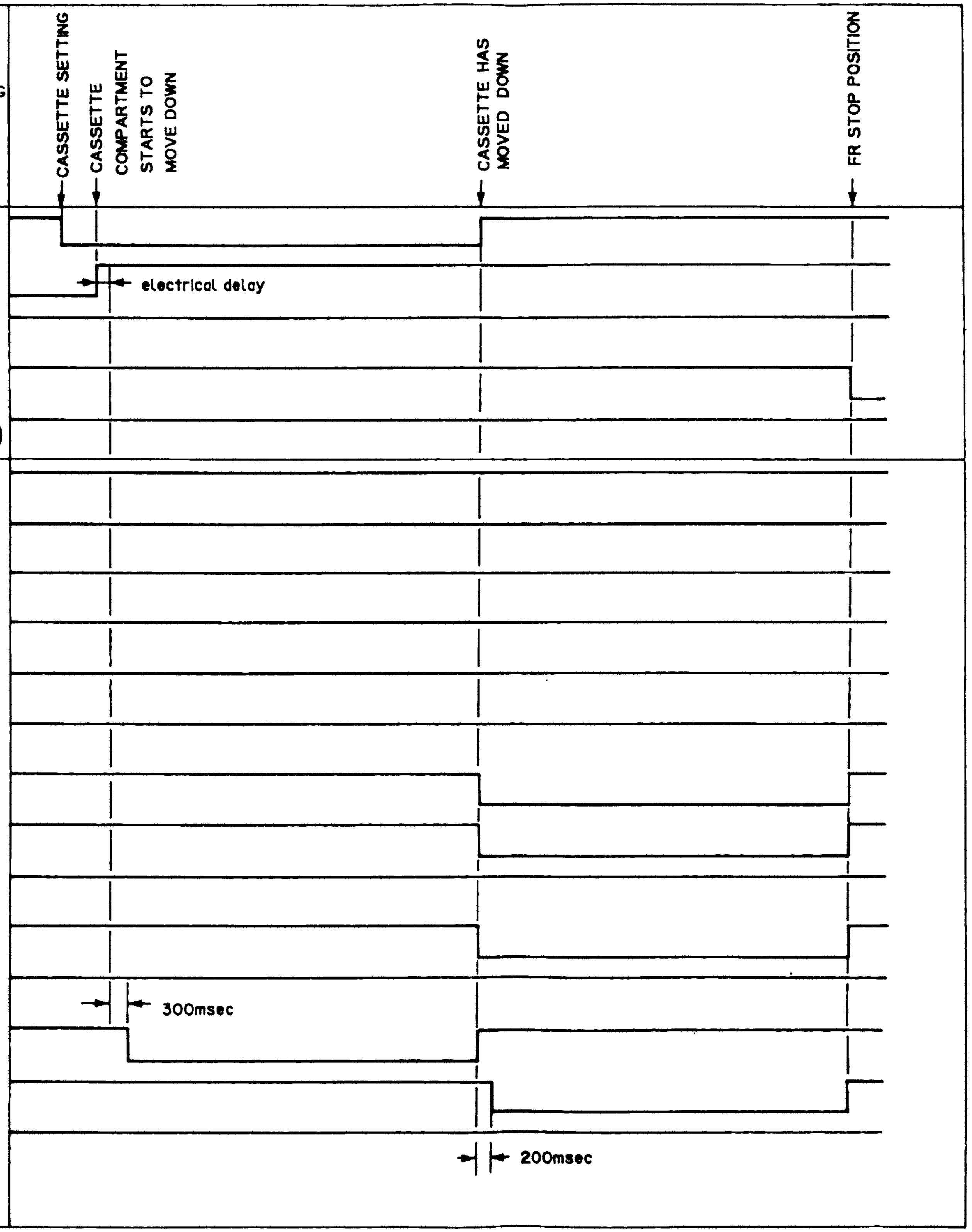
DATA DISPLAYED	CONDITION
0 0 0 0	REEL SLACK does not occur
0 1 1 0	FF or REW mode
0 1 1 1	FR-STOP → FR UNTHREAD
1 0 0 0	x1 NORMAL SPEED or less
1 0 0 1	Higher than x1 NORMAL SPEED
1 0 1 0	THREAD END → FR-STOP

NOTE 8 REMOTE CONTROL CODE

COMMAND	CODE	COMMAND	CODE
STOP	1 0 0 0	FWD SEARCH	0 1 1 0
FF	1 1 0 0	REV SEARCH	0 1 1 1
REW	1 0 1 1	PAUSE	1 0 0 1
PLAY	1 0 1 0	REC	1 1 1 0

1. THREADING OPERATION (CASSETTE IN→CASSETTE DOWN→THREAD→FR STOP POSITION)

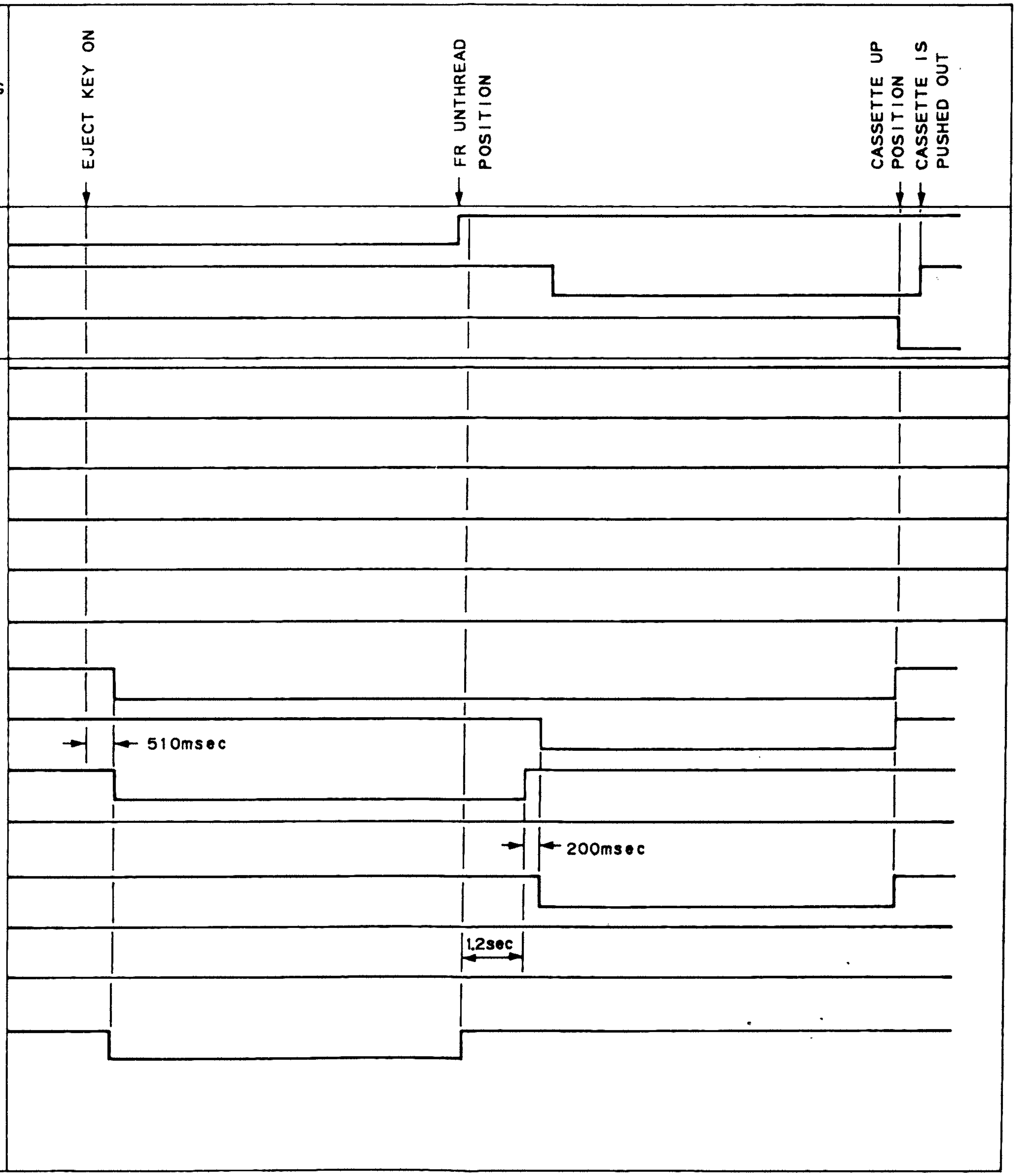
	SIGNAL	LABEL NUMBER ON DIAGNOSTICS	MEASURING POINT
INPUT	H : CASSETTE DOWN	08 — DIGIT 3	IC7-18
	H : CASSETTE IN	08 — DIGIT 4	IC7-17
	L : THREAD END	OL — DIGIT 3	IC7-5
	L : UNTHREAD END	OL — DIGIT 4	IC7-6
	L : DEW DET	14 — DIGIT 3	(IC1-35 KY-91)
OUTPUT	FWD / $\overline{\text{REV}}$	00 — DIGIT 1	IC7-41
	NORMAL / $\overline{\text{SEARCH}}$	00 — DIGIT 2	IC7-40
	H : DRUM STOP	01 — DIGIT 1	IC7-45
	L : SKEW SOL.ON	02 — DIGIT 2	IC7-48
	L : SEARCH SOL.ON	04 — DIGIT 2	IC7-23
	L : PINCH SOL.ON	04 — DIGIT 3	IC7-22
	L : T-BRAKE SOL.ON	05 — DIGIT 1	IC7-37
	L : S-BRAKE SOL.ON	05 — DIGIT 2	IC7-36
	L : T-IDLER SOL.ON	05 — DIGIT 3	IC7-35
	L : S-IDLER SOL.ON	05 — DIGIT 4	IC7-34
	L : C.C.UP	07 — DIGIT 1	IC7-16
	L : C.C. DOWN	07 — DIGIT 2	IC7-15
	L : THREAD MOTOR ON	07 — DIGIT 3	IC7-13
	L : UNTHREAD MOTOR ON	07 — DIGIT 4	IC7-14
			ON SY-51 BOARD



C.C. = CASSETTE UP COMPARTMENT

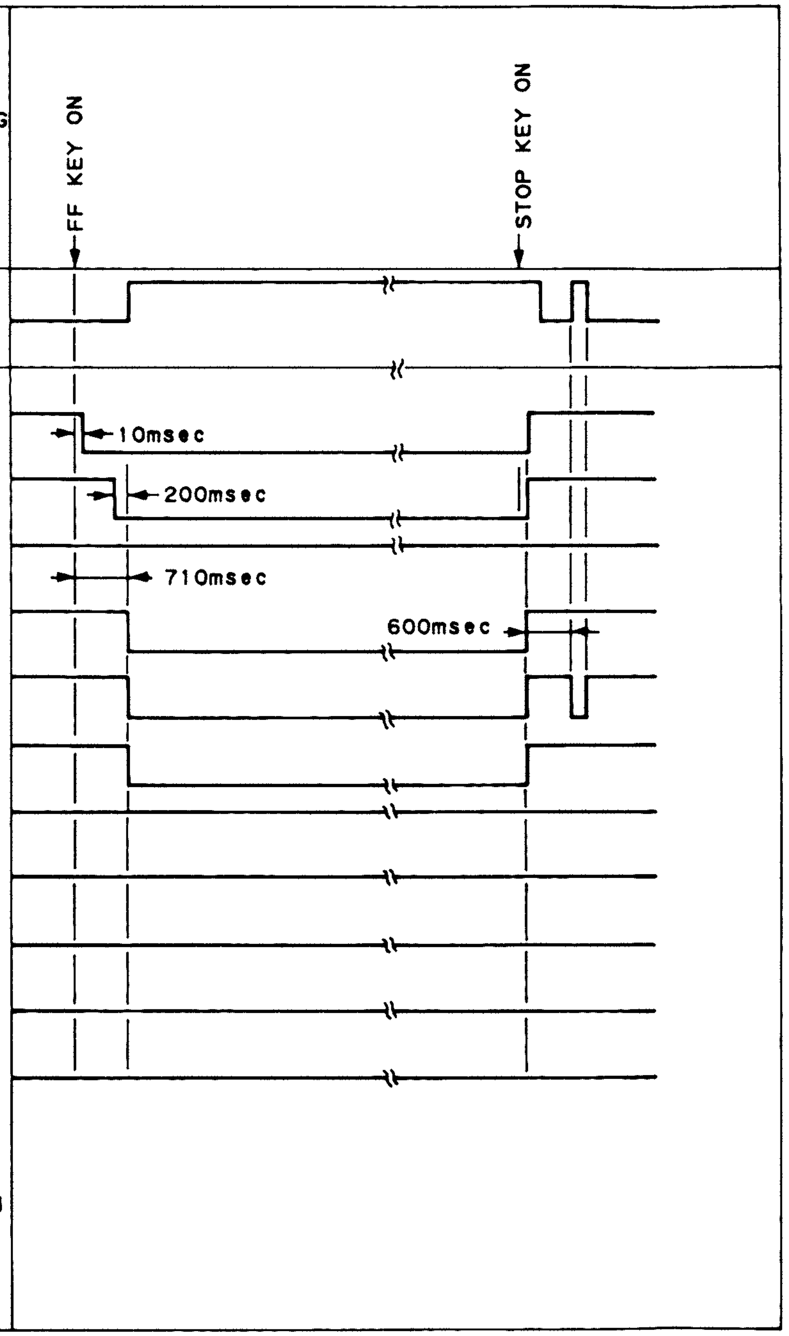
2. UNTHREADING OPERATION (FR STOP POSITION→FR UNTHREAD END POSITION→CASSETTE UP)

	SIGNAL	LABEL NUMBER ON DIAGNOSTICS	MEASURING POINT
INPUT	L : FR UNTHREAD END	08 — DIGIT 2	IC7-19
	H : CASSETTE DOWN	08 — DIGIT 3	IC7-18
	H : CASSETTE IN	08 — DIGIT 4	IC7-17
OUTPUT	FWD / $\overline{\text{REV}}$	00 — DIGIT 1	IC7-41
	NORMAL / $\overline{\text{SEARCH}}$	00 — DIGIT 2	IC7-40
	H : DRUM STOP	01 — DIGIT 1	IC7-45
	L : SKEW SOL.ON	02 — DIGIT 2	IC7-48
	L : SEARCH SOL.ON	04 — DIGIT 2	IC7-23
	L : PINCH SOL.ON	04 — DIGIT 3	IC7-22
	L : T-BRAKE SOL.ON	05 — DIGIT 1	IC7-37
	L : S-BRAKE SOL.ON	05 — DIGIT 2	IC7-36
	L : T-IDLER SOL.ON	05 — DIGIT 3	IC7-35
	L : S-IDLER SOL.ON	05 — DIGIT 4	IC7-34
	L : C.C.UP	07 — DIGIT 1	IC7-16
	L : C.C.DOWN	07 — DIGIT 2	IC7-15
	L : THREAD MOTOR ON	07 — DIGIT 3	IC7-13
	L : UNTHREAD MOTOR ON	07 — DIGIT 4	IC7-14
			ON SY-51 BOARD



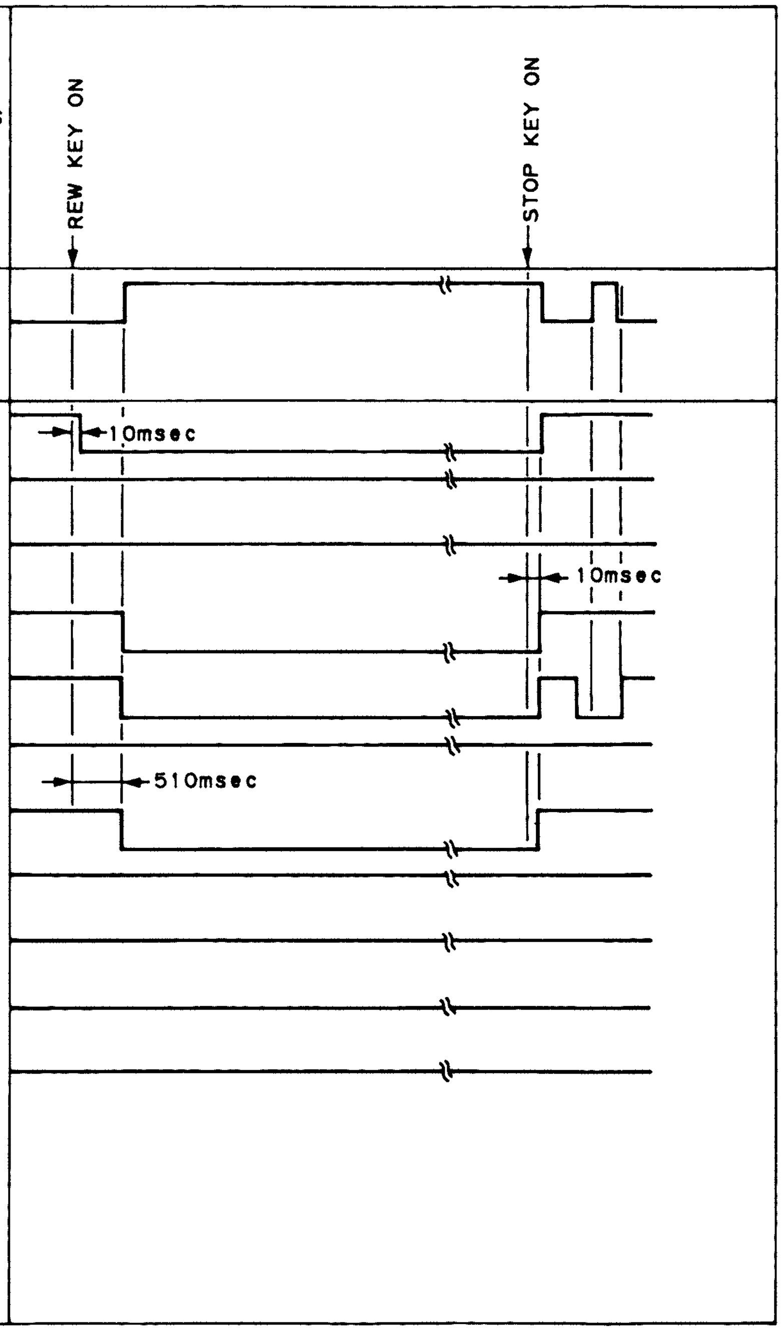
3. FF MODE (FR STOP→FF→FR STOP)

	SIGNRL	LABEL NUMBER ON DIAGNOSTICS	MEASURING POINT
INPUT	L : REEL STOP	09 — DIGIT 2	
OUTPUT	H : DRUM STOP	01 — DIGIT 1	IC7-45
	L : SEARCH SOL.ON	04 — DIGIT 2	IC7-23
	L : PINCH SOL.ON	04 — DIGIT 3	IC7-22
	L : T-BRAKE SOL.ON	05 — DIGIT 1	IC7-37
	L : S-BRAKE SOL.ON	05 — DIGIT 2	IC7-36
	L : T-IDLER SOL.ON	05 — DIGIT 3	IC7-35
	L : S-IDLER SOL.ON	05 — DIGIT 4	IC7-34
	L : C.C.UP	07 — DIGIT 1	IC7-16
	L : C.C.DOWN	07 — DIGIT 2	IC7-15
	L : THREAD MOTOR ON	07 — DIGIT 3	IC7-13
	L : UNTHREAD MOTOR ON	07 — DIGIT 4	IC7-14
			ON SY-51 BOARD



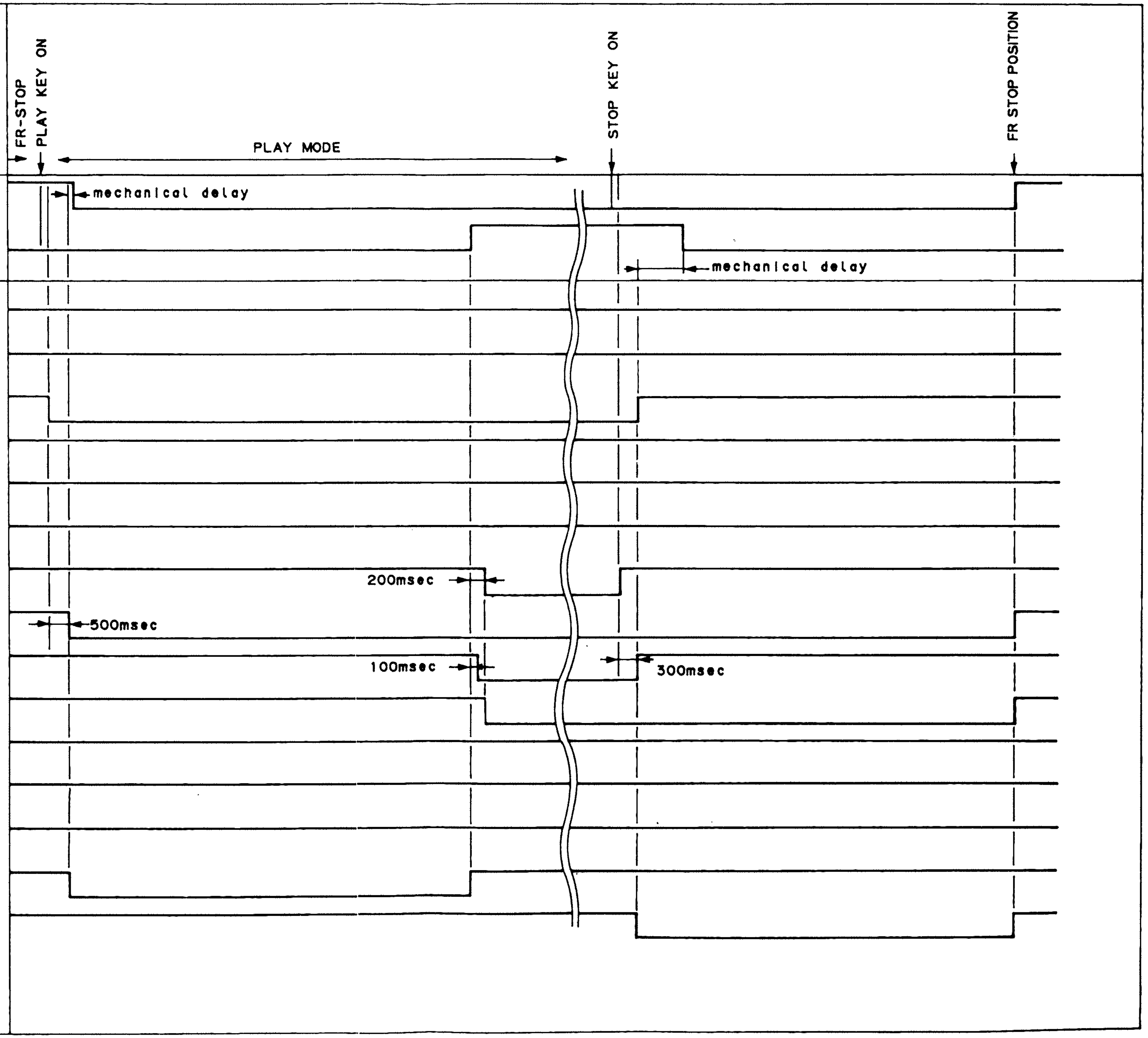
4. REW MODE (FR STOP→REW→FR STOP)

	SIGNAL	LABEL NUMBER ON DIAGNOSTICS	MEASURING POINT
INPUT	L : REEL STOP	09 — DIGIT 2	
OUTPUT	H : DRUM STOP	01 — DIGIT 1	IC7-45
	L : SEARCH SOL.ON	04 — DIGIT 2	IC7-23
	L : PINCH SOL.ON	04 — DIGIT 3	IC7-22
	L : T-BRAKE SOL.ON	05 — DIGIT 1	IC7-37
	L : S-BRAKE SOL.ON	05 — DIGIT 2	IC7-36
	L : T-IDLER SOL.ON	05 — DIGIT 3	IC7-35
	L : S-IDLER SOL.ON	05 — DIGIT 4	IC7-34
	L : C.C. UP	07 — DIGIT 1	IC7-16
	L : C.C. DOWN	07 — DIGIT 2	IC7-15
	L : THREAD MOTOR ON	07 — DIGIT 3	IC7-13
	L : UNTHREAD MOTOR ON	07 — DIGIT 4	IC7-14
			ON SY-51 BOARD



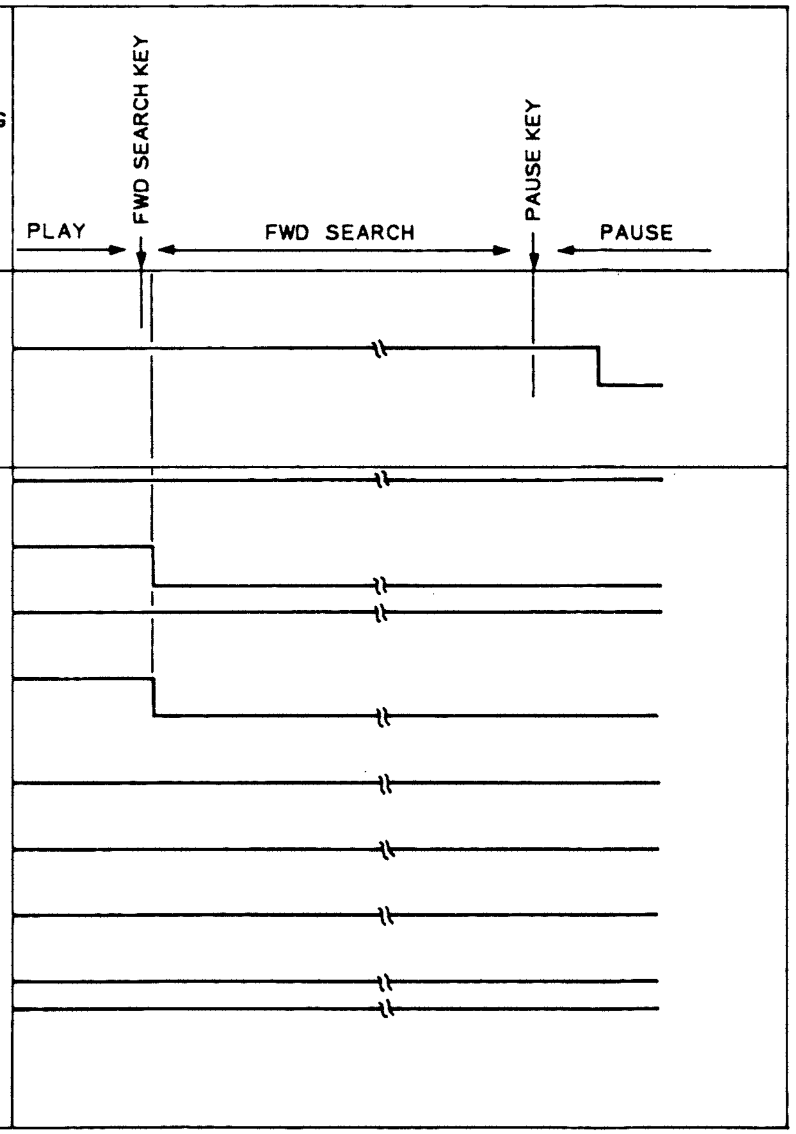
5. PLAY MODE (FR STOP→PLAY→FR STOP)

	SIGNAL	LABEL NUMBER ON DIAGNOSTICS	MEASURING POINT
INPUT	L : THREAD END	OL — DIGIT 3	IC7-5
	L : UNTHREAD END	OL — DIGIT 4	IC7-6
OUTPUT	FWD / $\overline{\text{REV}}$	00 — DIGIT 1	IC7-41
	NORMAL / $\overline{\text{SEARCH}}$	00 — DIGIT 2	IC7-40
	H : DRUM STOP	01 — DIGIT 1	IC7-45
	L : SKEW SOL.ON	02 — DIGIT 2	IC7-48
	H : REEL STILL	03 — DIGIT 3	IC7-58
	L : SEARCH SOL.ON	04 — DIGIT 2	IC7-23
	L : PINCHH SOL.ON	04 — DIGIT 3	IC7-22
	L : T-BRAKE SOL.ON	05 — DIGIT 1	IC7-37
	L : S-BRAKE SOL.ON	05 — DIGIT 2	IC7-36
	L : T-IDLER SOL.ON	05 — DIGIT 3	IC7-35
	L : S-IDLER SOL.ON	05 — DIGIT 4	IC7-34
	L : C.C UP	07 — DIGIT 1	IC7-16
	L : C.C DOWN	07 — DIGIT 2	IC7-15
	L : THREAD MOTOR ON	07 — DIGIT 3	IC7-13
	L : UNTHREAD MOTOR ON	07 — DIGIT 4	IC7-14
			ON SY-51 BOARD



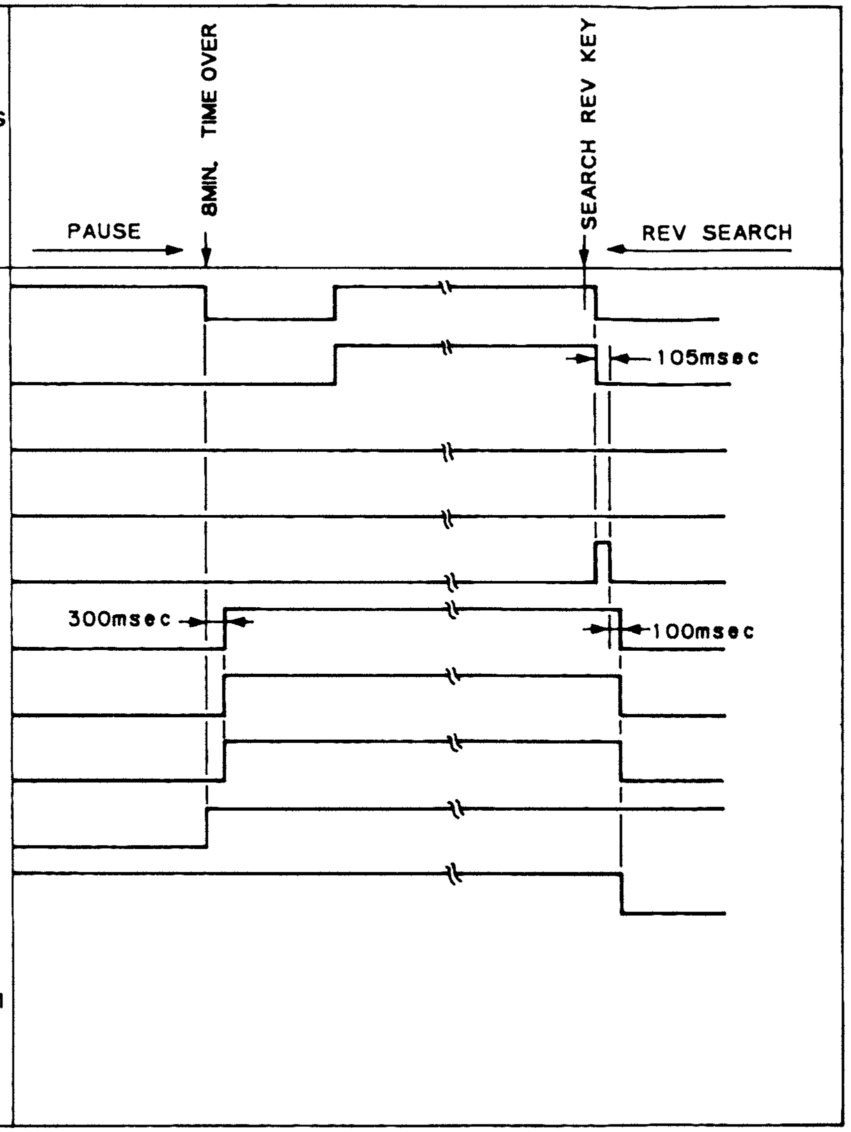
6. PLAY→FWD SEARCH→SEARCH PAUSE

	SIGNAL	LABEL NUMBER ON DIAGNOSTICS	MEASURING POINT
INPUT	L : CAPSTAN STOP	OL — DIGIT 1	IC7-8
OUTPUT	FWD / $\overline{\text{REV}}$	00 — DIGIT 1	IC7-41
	NORMAL / $\overline{\text{SEARCH}}$	00 — DIGIT 2	IC7-40
	H : REEL STILL	03 — DIGIT 3	IC7-58
	L : SEARCH SOL.ON	04 — DIGIT 2	IC7-23
	L : PINCH SOL.ON	04 — DIGIT 3	IC7-22
	L : T-BRAKE SOL.ON	05 — DIGIT 1	IC7-37
	L : S-BRAKE SOL.ON	05 — DIGIT 2	IC7-36
	L : T-IDLER SOL.ON	05 — DIGIT 3	IC7-35
	L : S-IDLER SOL.ON	05 — DIGIT 4	IC7-34
			ON SY-51 BOARD



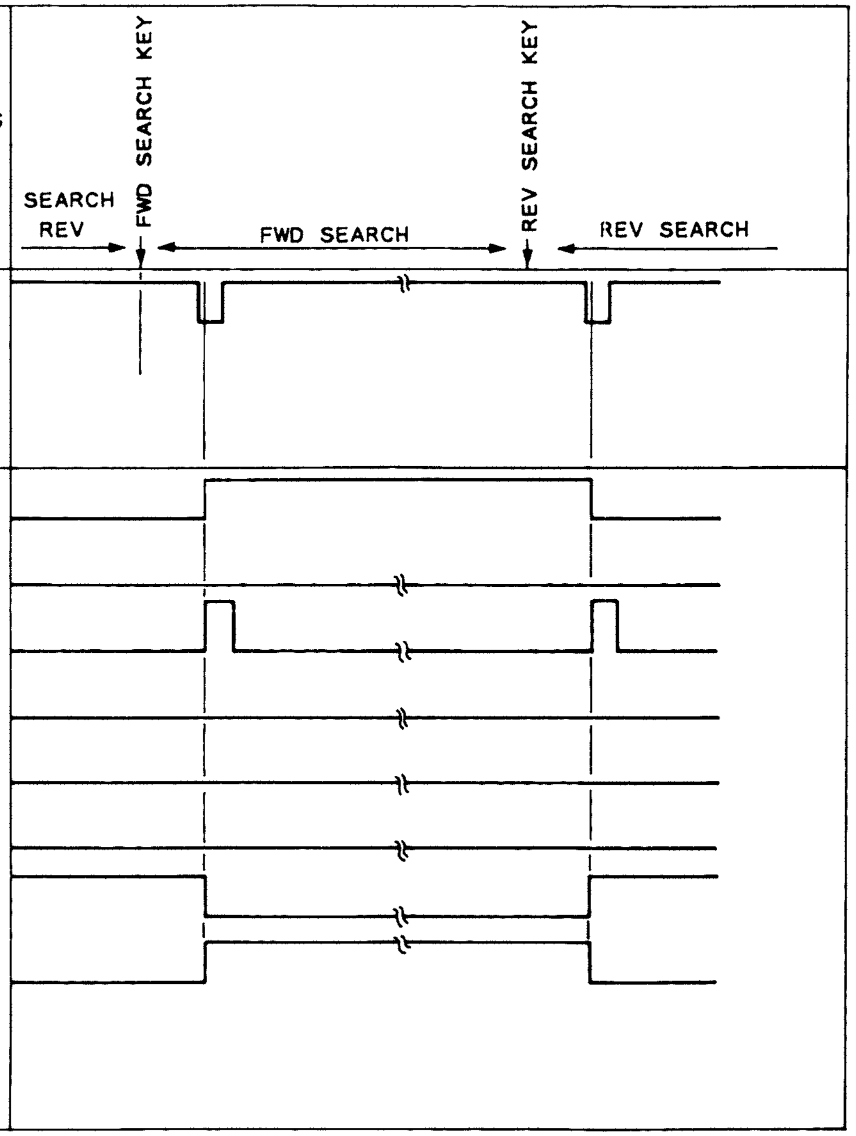
7. PLAY PAUSE→LONG PAUSE→REV SEARCH

	SIGNAL	LABEL NUMBER ON DIAGNOSTICS	MEASURING POINT
OUTPUT	FWD / $\overline{REV}$	00 — DIGIT 1	IC7-41
	NORMAL / $\overline{SEARCH}$	00 — DIGIT 2	IC7-40
	H : DRUM STOP	01 — DIGIT 1	IC7-45
	H : REEL STILL	03 — DIGIT 3	IC7-58
	L : SEARCH SOL.ON	04 — DIGIT 2	IC7-23
	L : PINCH SOL.ON	04 — DIGIT 3	IC7-22
	L : T-BRAKE SOL.ON	05 — DIGIT 1	IC7-37
	L : S-BRAKE SOL.ON	05 — DIGIT 2	IC7-36
	L : T-IDLER SOL.ON	05 — DIGIT 3	IC7-35
	L : S-IDLER SOL.ON	05 — DIGIT 4	IC7-34
			ON SY-51 BOARD



8. REV SEARCH→(FWD PAUSE)→FWD SEARCH→(FWD PAUSE)→REV SEARCH

	SIGNAL	LABEL NUMBER ON DIAGNOSTICS	MEASURING POINT
INPUT	L : CAPSTAN STOP	OL — DIGIT 1	IC7-8
OUTPUT	FWD / $\overline{\text{REV}}$	00 — DIGIT 1	IC7-41
	NORMAL / $\overline{\text{SEARCH}}$	00 — DIGIT 2	IC7-40
	H : REEL STILL	03 — DIGIT 3	IC7-58
	L : SEARCH SOL.ON	04 — DIGIT 2	IC7-23
	L : T-BRAKE SOL.ON	05 — DIGIT 1	IC7-37
	L : S-BRAKE SOL.ON	05 — DIGIT 2	IC7-36
	L : T-IDLER SOL.ON	05 — DIGIT 3	IC7-35
	L : S-IDLER SOL.ON	05 — DIGIT 4	IC7-34
			ON SY-51 BOARD



VP-5020(UC)
VP-5040(EK)
VP-5040(UC)
9-966-889-51

Sony Corporation

Printed in Japan
1986.10 08